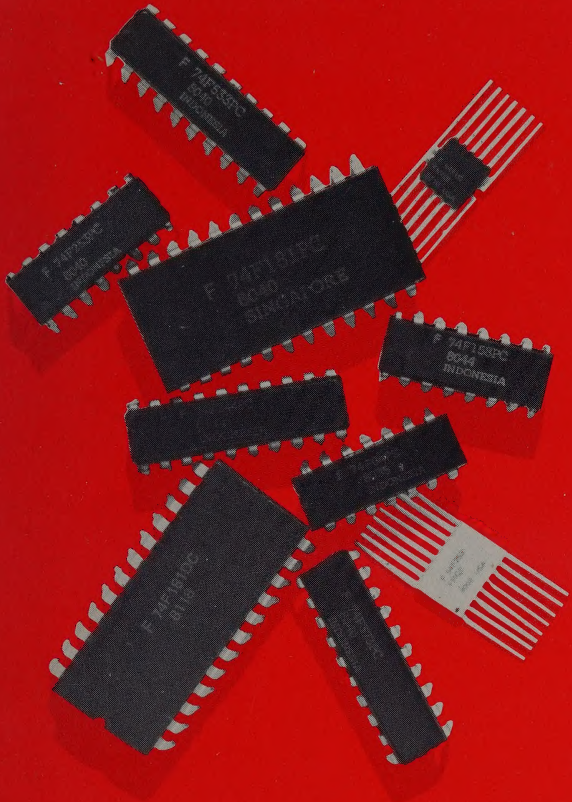
$3.95



FAST

Fairchild Advanced Schottky TTL

Pioneer
PIONEER-STANDARD ELECTRONICS, INC.
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DAYTON LOCAL - 236-9900 OHIO WATTS 800-762-7810
CIN. LOCAL - 628-1072 KY. WATTS 800-543-5113
COL. LOCAL - 221-0043 TWX 81-459-1622

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HANDLING PRECAUTIONS FOR SEMICONDUCTOR COMPONENTS

The following handling precautions should be observed for oxide isolation, shallow junction processed parts, such as FAST or 100K ECL:

1. All Fairchild devices are shipped in conducting foam or anti-static tubes. When they are removed for inspection or assembly, proper precautions should be used.

2. Fairchild devices, after removal from their shipping material, should be placed leads down on a grounded surface. Under no circumstances should they be placed in polystyrene foam or non-conducting plastic trays used for shipment and handling of conventional ICs.

3. Individuals and tools should be grounded before coming in contact with these devices.

4. Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn-on or off, do not exceed maximum ratings.

5. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{CC}, GND or the output of a logic element.

6. After assembly on PC boards, ensure that static discharge cannot occur during handling, storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam.

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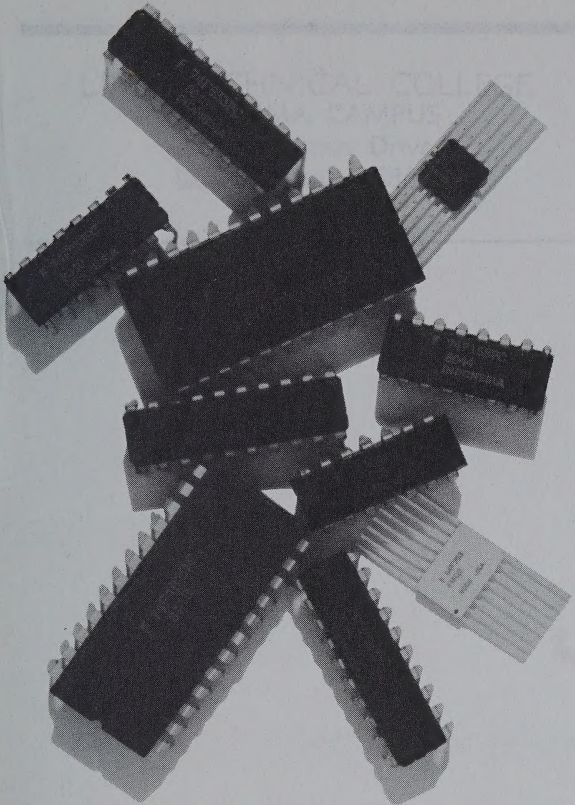

FAST

Fairchild Advanced Schottky TTL

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Digital Products Division
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207/775-8100 • Telex 710-221-1980

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Introduction

Fairchild Advanced Schottky TTL, FAST, is a family of TTL circuits that exhibits a combination of performance and efficiency unapproached by any other TTL family. Made with the proven Isoplanar process, 54F/74F circuits offer the switching speed and output drive capability of Schottky TTL, with superior noise margins and only one-fourth the power consumption.

Section 1 Product Index and Selection Guide
Lists 54F/74F circuits currently available, in design or planned. The Selection Guide groups the circuits by function.

Section 2 Circuit Characteristics
Discusses FAST technology, circuit configurations and characteristics.

Section 3 Ratings, Specifications and Waveforms
Contains common ratings and specifications for FAST devices, as well as ac test load and waveforms.

Section 4 Data Sheets
Contains data sheets for currently available and pending new products.

Section 5 New Products
Contains brief descriptions of new products currently planned.

Section 6 Ordering Information and Package Outlines
Explains simplified purchasing code which identifies not only device type but also the package type and temperature range. Contains detailed physical dimension drawings for each package.

Section 7 Field Sales Offices, Representatives and Distributor Locations

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Section 6 Ordering Information and Package Outlines

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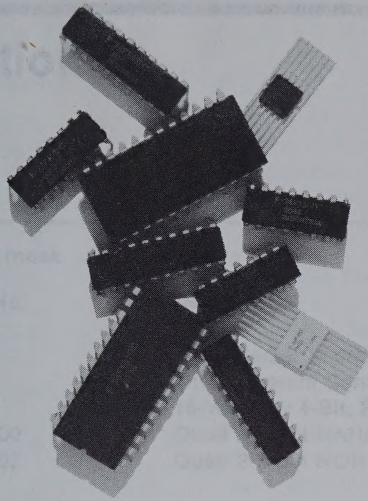
*Also shown on inside back cover.



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Circuit Characteristics 2

Ratings, Specifications and Waveforms 3

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New Products 5

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Section 1

Product Index and Selection Guide

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Selection Guide

Gates

Function	Device No.	Page No.	Function	Device No.	Page No.
NAND			*OR/NOR/Exclusive-OR*		
Quad 2-Input	54F/74F00	4-3	Quad 2-Input OR	54F/74F32	4-10
Triple 3-Input	54F/74F10	4-7	Quad 2-Input NOR	54F/74F02	4-4
Dual 4-Input	54F/74F20	4-9	Quad 2-Input Exclusive-OR	54F/74F86	4-15
AND			*Invert/AND-OR-Invert*		
Quad 2-Input	54F/74F08	4-6	Hex Inverter	54F/74F04	4-5
Triple 3-Input	54F/74F11	4-8	AND-OR-Invert	54F/74F64	4-11

Dual Edge-Triggered Flip-Flops

Function	Device No.	Inputs	Clock Edge	Direct Set	Direct Clear	Maximum Clock Frequency @25°C MHz (Min)	Page No.
Dual D	54F/74F74	D	↑	Yes	Yes	100	4-12
Dual J$\overline{K}$	54F/74F109	J,$\overline{K}$	↑	Yes	Yes	90	4-16
Dual JK	54F/74F112	J,K	↓	Yes	Yes	100	4-19
Dual JK	54F/74F113	J,K	↓	Yes	No	100	4-22
Dual JK	54F/74F114	J,K	↓	Yes	Yes	100	4-25

Multiple Flip-Flop/Registers

Function	Device No.	Data Inputs	Common Clear (Level)	CP Inputs (Level)	Maximum Clock Frequency @25°C MHz (Min)	Page No.
4-Bit D Flip-Flop	54F/74F175	4 x D	1(L)	1 (↑)	100	4-68
4-Bit D Flip-Flop	54F/74F379	4 x D		1 (↑)	100	4-167
6-Bit D Flip-Flop	54F/74F174	6 x D	1(L)	1 (↑)	100[2]	4-65
6-Bit D Flip-Flop	54F/74F378	6 x D		1 (↑)	100[2]	4-164
8-Bit D Flip-Flop (3S)[1]	54F/74F374	8 x D		1 (↑)	100	4-162
8-Bit D Flip-Flop (3S)[1]	54F/74F534	8 x D		1 (↑)	100	4-203
Dual 8-Bit Register (3S)[1]	54F/74F604	2(8 x D)		1 (↑)	NA	5-18
Dual 8-Bit Register (OC)[1]	54F/74F605	2(8 x D)		1 (↑)	NA	5-18
Dual 8-Bit Register (3S)[1]	54F/74F606	2(8 x D)		1 (↑)	NA	5-18
Dual 8-Bit Register (OC)[1]	54F/74F607	2(8 x D)		1 (↑)	NA	5-18
Quad 2-Port Register	54F/74F398	2(4 x D)		1 (↑)	100	4-188
Quad 2-Port Register	54F/74F399	2(4 x D)		1 (↑)	100	4-188
Octal Registered Transceiver (3S)[1]	54F/74F550	2(8 x D)		2 (↑)		4-229
Octal Registered Transceiver (3S)[1]	54F/74F551	2(8 x D)		2 (↑)		4-229

1. 3S = 3-state
2. Preliminary
3. NA = Data not available

Selection Guide (Cont'd)

Latches

Function	Device No.	Data Inputs	Common Clear (Level)	Enable Inputs (Level)	Enable Pulse Width @25°C ns (Min)	Enable to Output Delay @25°C ns (Max)	Page No.
Octal D (3S)*	54F/74F373	8 x D		1 (H)	6.0	11.5	4-159
Octal D (3S)*	54F/74F533	8 x D		1 (H)	6.0	11	4-201
Octal D (3S)* w/Interrupt	54F/74F412	8 x D	1 (L)				5-10
Octal D (3S)* w/Interrupt	54F/74F432	8 x D	1 (L)				5-13
Octal D Registered Transceiver (3S)*	54F/74F543	2(8 x D)		2 (L)		12**	4-215
Octal D Registered Transceiver (3S)*	54F/74F544	2(8 x D)		2 (L)		12**	4-215

Multiplexers

Function	Device No.	Enable Inputs (Level)	True Output	Complement Output	Page No.
4-Input (3S)*	54F/74F350	1 (L)	Yes	No	4-149
8-Input	54F/74F151	1 (L)	Yes	Yes	4-38
8-Input (3S)	54F/74F251	1 (L)	Yes	Yes	4-112
Dual 4-Input	54F/74F153	2 (L)	Yes	No	4-41
Dual 4-Input (3S)*	54F/74F253	2 (L)	Yes	No	4-115
Dual 4-Input	54F/74F352	2 (L)	No	Yes	4-153
Dual 4-Input (3S)*	54F/74F353	2 (L)	No	Yes	4-156
Quad 2-Input	54F/74F157	1 (L)	Yes	No	4-44
Quad 2-Input	54F/74F158	1 (L)	No	Yes	4-47
Quad 2-Input (3S)*	54F/74F257	1 (L)	Yes	No	4-118
Quad 2-Input (3S)*	54F/74F258	1 (L)	No	Yes	4-121
Quad 2-Input	54F/74F398		Yes	Yes	4-188
Quad 2-Input	54F/74F399		Yes	No	4-188

Decoders/Demultiplexers

Function	Device No.	Address Inputs	Active-LOW Enable	Active-HIGH Enable	Active-LOW Output Enable	Active-LOW Outputs	Active-HIGH Outputs	Page No.
Dual 1-of-4	54F/74F139	2 + 2	1 + 1			4 + 4		4-31
Dual 1-of-4 (3S)*	54F/74F539	2 + 2	1 + 1		1 + 1		4 + 4	4-212
1-of-8	54F/74F138	3	2	1		8		4-28
1-of-8 (3S)*	54F/74F538	3	2	2	2		8	4-209
1-of-8 w/Address Latches	54F/74F547	3	1	2		8		4-222
1-of-8	54F/74F548	3	2	2		8		4-226
1-of-10 (3S)*	54F/74F537	4	1	1	1		10	4-206

*3S = 3-State; OC = Open-collector
** Preliminary

Selection Guide (Cont'd)

Shift Registers/FIFOs

Function	Device No.	No. of Bits	Serial Entry	Clock Edge	Maximum Clock Frequency @25°C MHz (Min)	Page No.
Shift Right, Serial-in/Parallel-out	54F/74F164	8	2		80	4-58
Shift Right, Serial/Parallel-in, Parallel/Serial-out (3S)[1]	54F/74F322	8	2		70[3]	4-141
Shift Right, Serial-in, Serial/Parallel-out	54F/74F673	16	1		100[3]	4-250
Shift Right, Serial/Parallel-in, Serial-out	54F/74F674	16	1		100[3]	4-254
Shift Right, Serial-in, Serial/Parallel-out	54F/74F675	16	1		100[3]	4-257
Shift Right, Serial/Parallel-in, Serial-out	54F/74F676	16	1		100[3]	5-24
Bidirectional, Serial/Parallel-in, Parallel/Serial-out	54F/74F194	4	2		105	4-99
Bidirectional, Serial/Parallel-in, Parallel/Serial-out (3S)[1]	54F/74F299	8	2		70[3]	4-134
Bidirectional, Serial/Parallel-in, Parallel/Serial-out (3S)[1]	54F/74F323	8	2		70[3]	4-145
16 x 4 FIFO, Serial/Parallel-in, Serial/Parallel-out (3S)[1]	54F/74F403	4	1			5-10
64 x 4 FIFO, Parallel-in/Parallel-out	54F/74F413	4				5-11
64 x 4 FIFO, Serial/Parallel-in, Serial/Parallel-out (3S)[1]	54F/74F433	4	1			5-14

Synchronous Presettable Counters

Function	Device No.	Modulus	No. of Bits	Parallel Entry[2]	Maximum Clock Frequency @25°C MHz (Min)	Page No.
BCD Count-Up	54F/74F160	10	4	S	100[3]	4-50
BCD Count-Up	54F/74F162	10	4	S	100[3]	4-50
BCD Up-Down	54F/74F168	10	4	S	75[3]	4-61
BCD Up-Down	54F/74F190	10	4	A	80	4-82
BCD Up-Down	54F/74F192	10	4	A	80[3]	4-91
BCD Up-Down (3S)[1]	54F/74F568	10	4	S	75[3]	4-240
Binary Count-Up	54F/74F161	16	4	S	100[3]	4-54
Binary Count-Up	54F/74F163	16	4	S	100[3]	4-54
Binary Up-Down	54F/74F169	16	4	S	75[3]	4-61
Binary Up-Down	54F/74F191	16	4	A	80	4-86
Binary Up-Down	54F/74F193	16	4	A	80	4-95
Binary Up-Down (3S)[1]	54F/74F569	16	4	S	75[3]	4-240
Binary Up-Down	54F/74F269	256	8	S	100[3]	5-7
Binary Up-Down (3S)[1]	54F/74F579	256	8	S	100[3]	5-16
Binary Up-Down (3S)[1]	54F/74F779	256	8	S	100[3]	5-25

1. (3S) = 3-state
2. S = Synchronous; A = Asynchronous
3. Preliminary

3-State Buffer/Line Driver/Transceivers

Function	Device No.	Enable Inputs (Level)	Current Sinking Side A/Side B mA	Page No.
Octal Buffer/Line Driver	54F/74F240	2(L)	64	4-105
Octal Buffer/Line Driver	54F/74F241	1(L) + 1(H)	64	4-105
Octal Buffer/Line Driver	54F/74F244	2(L)	64	4-105
Quad Bus Transceiver	54F/74F242	1(L) + 1(H)	64/64	4-107
Quad Bus Transceiver	54F/74F243	1(L) + 1(H)	64/64	4-107
Octal Bus Transceiver	54F/74F245	1(L)	20/64	4-110
Octal Bus Transceiver	54F/74F545	1(L)	20/64	4-219
Octal Registered Transceiver	54F/74F543	2(L)	20/64	4-215
Octal Registered Transceiver	54F/74F544	2(L)	20/64	4-215
Octal Registered Transceiver	54F/74F550	2(L)	20/64	4-229
Octal Registered Transceiver	54F/74F551	2(L)	20/64	4-229
GPIB Octal Transceiver	54F/74F588	1(L)	20/64	4-247

Arithmetic Operators

Function	Device No.	Description	No. of Bits	Page No.
Adder	54F/74F283	Full Binary 4-Bit with Fast Carry	4	4-127
Adder	54F/74F583	Full BCD with Fast Carry	4	5-17
Adder/Subtractor	54F/74F385	Quad Serial with Carry-Save	4 x 1	4-185
Adder/Subtractor	54F/74F582	BCD Add/Subtract/Compare with Ripple and Lookahead Carry	4	5-17
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Arithmetic Logic Unit	54F/74F181	ALU with Ripple and Lookahead Carry	4	4-71
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Carry Lookahead	54F/74F182	CLA for 4 ALUs		4-75
Comparator	54F/74F521	8-Bit Equality Comparator	2 x 8	4-192
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*3S = 3-State; OC = Open-collector

Selection Guide (Cont'd)

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16 x 4 RAM (OC)*	54F/74F319	18**	8.0**	4-138
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16 x 9 RAM w/Latch (3S)*	54F/74F211	15**	8.0**	5-5
16 x 9 RAM (OC)*	54F/74F312	15**	8.0**	5-8
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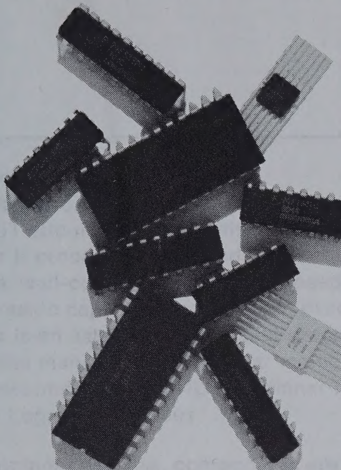
Microprogram Controller	29F10	5-4

*3S = 3-State; OC = Open-collector
** Preliminary



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Section 2 Circuit Characteristics

FAST Technology

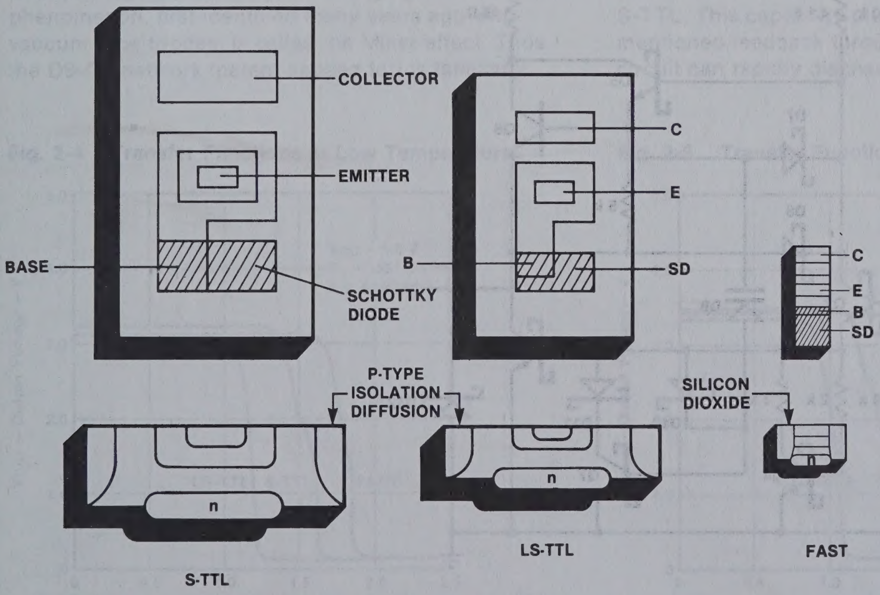
FAST is an acronym for Fairchild Advanced Schottky TTL. FAST circuits are made with the advanced Isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz. Isoplanar is an established Fairchild process, used for years in the manufacture of bipolar memories, CMOS, subnanosecond ECL and I^3L™ (Isoplanar Integrated Injection Logic) LSI devices.

In the Isoplanar process, components are isolated by a selectively grown thick oxide rather than the P^+ isolation region used in the Planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

Figure 2-1 shows the relative size of phase-splitter transistors (Q2 in *Figure 2-3*) used in Schottky, Low Power Schottky and FAST circuits. The LS-TTL transistor is smaller than that of S-TTL because of process refinements, shallower diffusions and smaller operating currents. The relative size of the FAST transistor illustrates the remarkable reduction afforded by the Isoplanar process. This in turn reduces junction capacitances, while the oxide isolation reduces sidewall capacitance. The effect of these reductions is an increase in frequency response by a factor of three or more. *Figure 2-2* shows the frequency response of two sizes of transistors made with the Isoplanar II process. Because they have modest, well-defined loads and thus can use smaller, faster transistors, internal gates of MSI devices are faster than SSI gates such as the 74F00 or 74F02. SSI gates, on the other hand, are designed to have high output drive capability and thus use larger transistors.

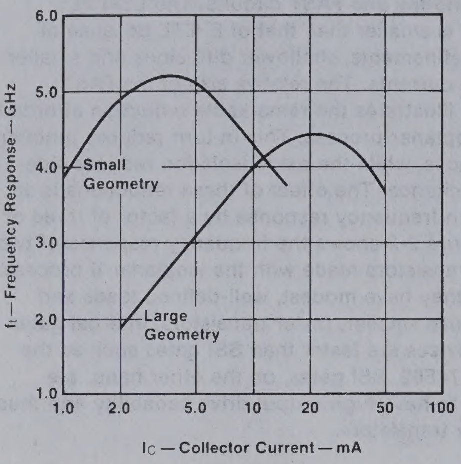
As is the case with other modern LSI processes, the shallower diffusions and thinner oxides make FAST

Fig. 2-1 Relative Transistor Sizes in Various TTL Families



devices more susceptible to damage from electrostatic discharge than are devices of earlier TTL families. Users should take the usual precautions when handling FAST devices: avoid placing them on non-conductive plastic surfaces or in plastic bags, make sure test equipment and jigs are grounded, individuals should be grounded before handling the devices, etc.

Fig. 2-2 Isoplanar Transistor Frequency Response

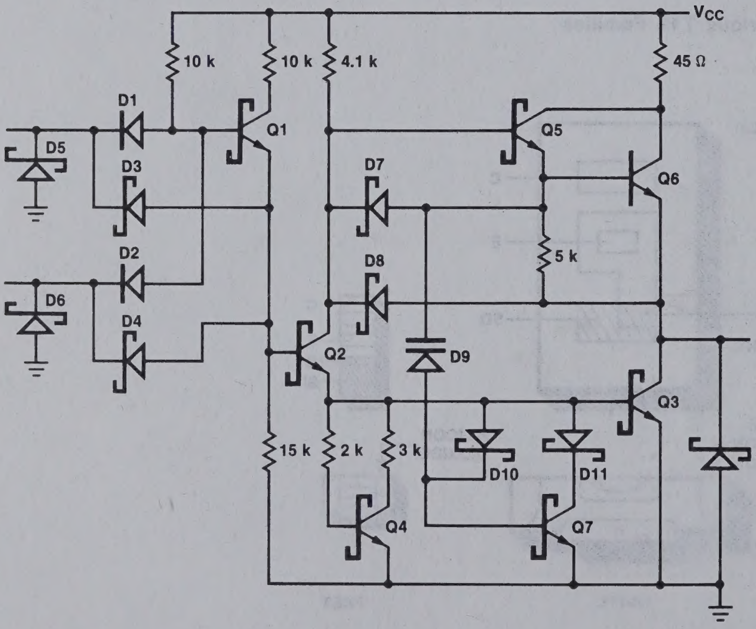


FAST Circuitry

The 2-input NAND gate, shown in *Figure 2-3*, has three stages of gain (Q1, Q2, Q3) instead of two stages as in other TTL families. This raises the input threshold voltage and increases the output drive. The higher threshold makes it possible to use pn diodes for the input AND function (D1 and D2) and still achieve an input threshold of 1.5 V. The capacitance of these diodes is comparatively low, which results in improved ac noise immunity. The effect of the threshold adjustment can be seen in the voltage transfer characteristics of *Figure 2-4, 2-5* and *2-6*. At 25°C (*Figure 2-5*) the FAST circuit threshold is nearly centered between the 0.8 V and 2.0 V limits specified for TTL circuits. This gives a better balance between the HIGH- and LOW-state noise margins. The +125°C characteristics (*Figure 2-6*) show that the FAST circuit threshold is comfortably above the 0.8 V specification, more so than in S-TTL or LS-TTL circuits. At –55°C, the FAST circuit threshold is still well below the 2.0 V specification, as shown in *Figure 2-4*.

FAST circuits contain several speed-up diodes to help discharge internal capacitances. Referring again to *Figure 2-3*, when a HIGH-to-LOW transition occurs at the D1 input, for example, Schottky diode D3 acts as a low-resistance path to discharge the several parasitic capacitances connected to the base of Q2. This effect

Fig. 2-3 Basic FAST Gate Schematic



only comes into play, however, as the input signal falls below about 1.2 V; D3 does not act as an entry path for negative spikes superimposed on a HIGH input level. When Q2 turns on and its collector voltage falls, D7 provides a discharge path for capacitance at the base of Q6. Whereas D3, D4 and D7 enhance switching speed by helping to discharge internal nodes, D8 contributes to the ability of a FAST circuit to rapidly discharge load capacitance. Part of the charge stored in load capacitance passes through D8 and Q2 to increase the base current of Q3 and increase Q3's current sinking capability during the HIGH-to-LOW output voltage transition.

In addition to the 2K-Q4-3K squaring network, which is standard for Schottky-clamped TTL circuits, FAST circuits contain a network D9-D10-D11-Q7 whose purpose is to provide a momentary low impedance at the base of Q3 during an output LOW-to-HIGH transition. The rising voltage at the emitter of Q5 causes displacement current to flow through varactor diode D9 and momentarily turn on Q7, which in turn pulls down the base of Q3 and absorbs the displacement current that flows through the collector-base capacitance (not shown) of Q3 when the output voltage rises. Without the D9-Q7 network, the displacement current through the collector-base capacitance acts as base current, tending to prolong the turn-off of Q3 and allow current to flow from Q6 to ground through Q3.

The collector-base capacitance of Q3, although small, is effectively multiplied by the voltage gain of Q3. This phenomenon, first identified many years ago with vacuum tube triodes, is called the Miller effect. Thus the D9-Q7 network (patent applied for) is familiarly called the "Miller killer" circuit and its use improves the output rise time and minimizes power consumption during repetitive switching at high frequencies. Diode D10 completes the discharge path for D9 through D7 when Q2 turns on. D11 limits how low Q7 pulls down the base of Q3 to a level adequate for the intended purpose, without sacrificing turn-on speed when a circuit is cycled rapidly.

Also shown in *Figure 2-3* is a clamp diode D12 at the output. This diode limits negative voltage excursions due to parasitic coupling in signal lines or transmission line effects.

The Schottky clamping diodes built into the transistors prevent saturation, thereby eliminating storage time as a factor in switching speed. Similarly, the speed-up diodes tend to minimize the impact of other variables on switching speed. The overall effect is to minimize variation in switching speed of FAST circuits with variations in supply voltage and ambient temperature (*Figures 2-7* and *2-8*). Propagation delay is specified not only under nominal supply voltage and temperature conditions, but also over the recommended operating range of V_{CC} and T_A for both military and commercial grade devices.

The internal switching speed of a logic circuit is only one aspect of the circuit's suitability for high-speed operation at the system or subsystem level; the other aspect is the ability of the circuit to drive load capacitance. FAST circuit outputs are structured to sink at least 20 mA in the LOW state, the same as S-TTL. This capability plus the effect of the aforementioned feedback through D8 assures that the circuit can rapidly discharge capacitance. During a

Fig. 2-4 Transfer Functions at Low Temperature

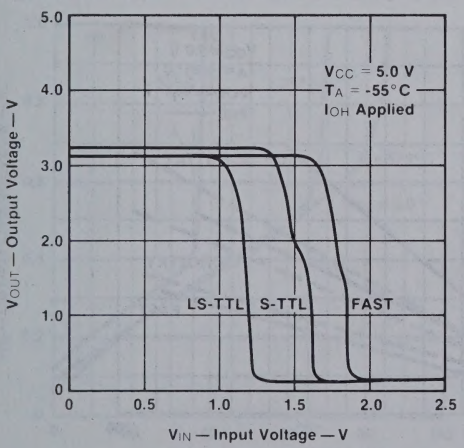
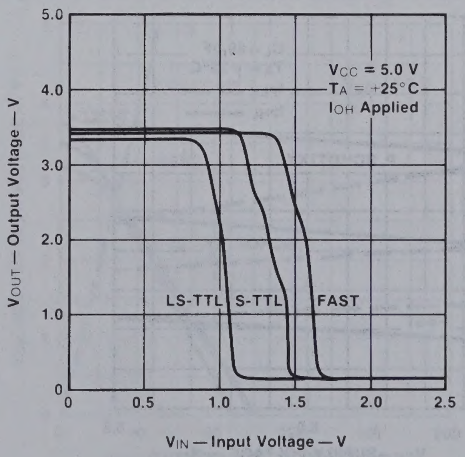


Fig. 2-5 Transfer Functions at Room Temperature



LOW-to-HIGH transition, the pull-up current is limited by the 45 Ω resistor, versus 55 Ω for S-TTL. Therefore, FAST circuits are inherently more capable than S-TTL of charging load capacitance.

Figure 2-9 shows the effects of load capacitance on propagation delays of FAST, S-TTL and LS-TTL NAND gates. The curves show that FAST gates are not only faster than those of earlier families, but also are less affected by capacitance and exhibit less skew between the LOW-to-HIGH and HIGH-to-LOW delays. These improved characteristics offered by FAST circuits make it easier to predict system performance early in the design phase, before loading details are precisely known. The curves show that the skew between HIGH-to-LOW and LOW-to-HIGH delays for the FAST gate is only about 0.5 ns, over a broad range of load capacitance, whereas the skew for the S-TTL gate is 1 ns or greater, depending on loading.

Output Characteristics

Figure 2-10 shows the current-voltage characteristics of a FAST gate with the pull-down transistor Q3 turned on. These curves illustrate instantaneous conditions in discharging load capacitance during an output HIGH-to-LOW transition. When the output voltage is at about 3.5 V, for example, the circuit can absorb charge from the load capacitance at a 500 mA rate at +25°C. From this level the rate decreases steadily down to about 100 mA at 1.5 V. In this region from 3.5 V to 1.5 V, part of the charge from the load capacitance is fed back through D8 (*Figure 2-3*) and Q2 to provide extra base

Fig. 2-6 Transfer Functions at High Temperature

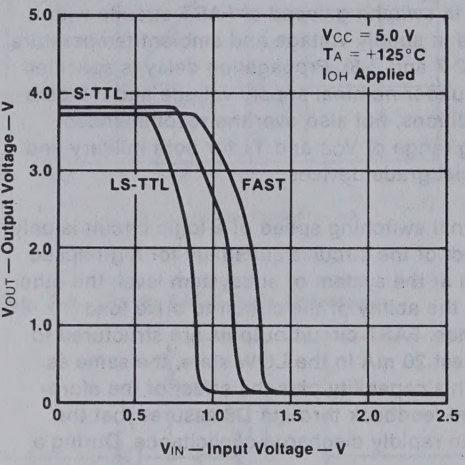


Fig. 2-7 Propagation Delay vs V_{CC}

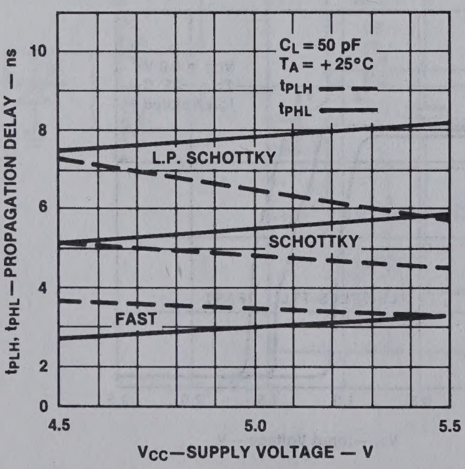


Fig. 2-8 Propagation Delay vs Temperature

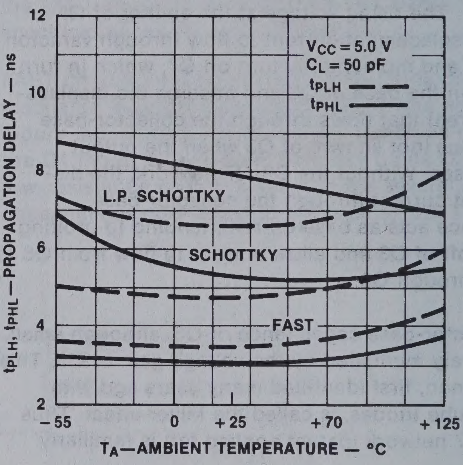
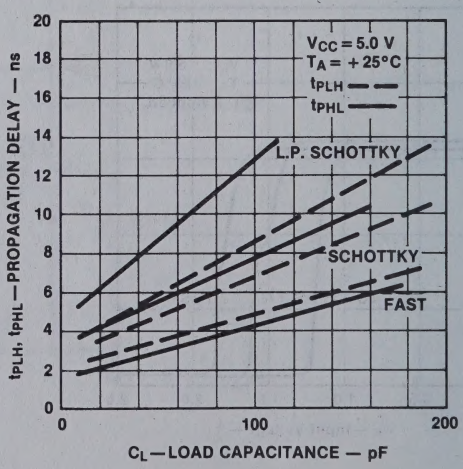


Fig. 2-9 Propagation Delay vs Load Capacitance



current for Q3, boosting its current-sinking capability and thus reducing the fall time. Below the 1.5 V level, Q3 continues to discharge the load capacitance, but without extra base current from D8. At about 0.5 V the integral Schottky clamp diode from base to collector of Q3 starts conducting and prevents Q3 from going into deep saturation.

On a greatly expanded scale, the output LOW characteristics of a gate are shown in *Figure 2-11*. With no load, the output voltage is about 0.1 V, increasing with current on a slope of about 7.5 Ω. When the load current increases beyond the current-sinking capability of Q3, the output voltage rises steeply. It can be seen that the worst-case specification of 0.5 V max at 20 mA load is easily met. Similar characteristics for a buffer are shown in *Figure 2-12*, over a broader current range. The curves are well below the output LOW voltage specification of 0.55 V max at 48 mA over the Military temperature range or 64 mA over the Commercial temperature range.

The output HIGH characteristics of a FAST gate are shown in *Figure 2-13*. At low values of output current the voltage is approximately 3.5 V. This value is just the supply voltage minus the combined base-emitter voltages of the Darlington pull-up transistors Q5 and Q6 (*Figure 2-3*). For load currents above 16 or 18 mA, the voltage drop across the 45 Ω Darlington collector resistor becomes appreciable and the Darlington saturates. For greater load currents the output voltage decreases with a slope of about 50 Ω, which is largely

Fig. 2-10 Output LOW Characteristics — 'F00

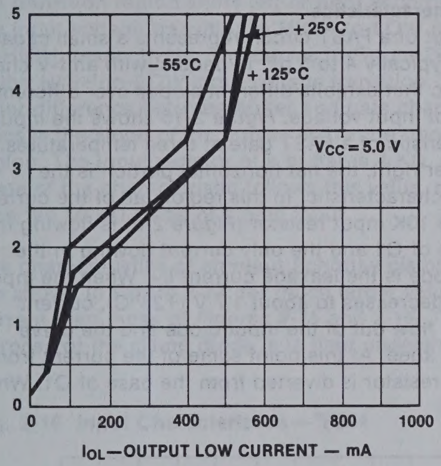


Fig. 2-12 Output LOW Characteristics — 'F244

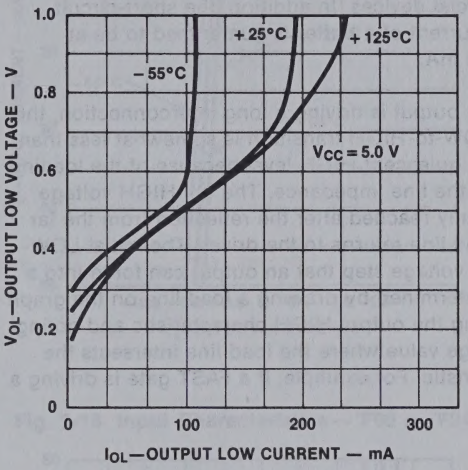


Fig. 2-11 Output LOW Characteristics — 'F00

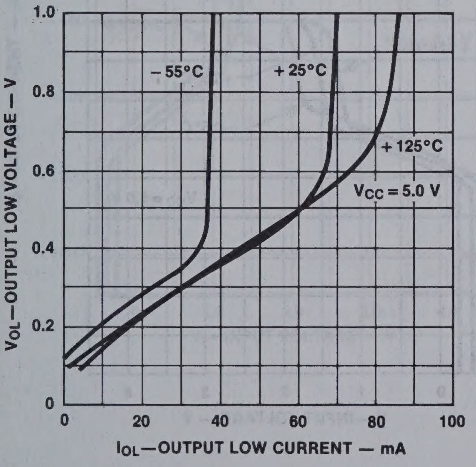
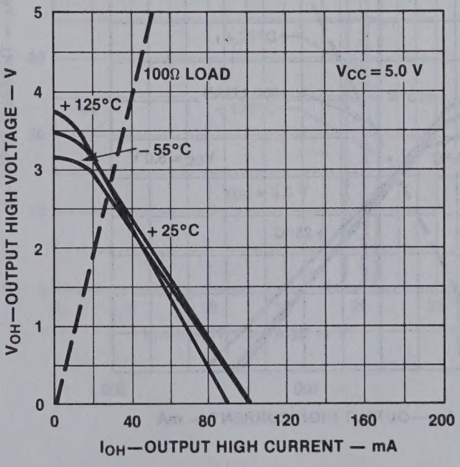


Fig. 2-13 Output HIGH Characteristics — 'F00



due to the 45 Ω resistor. The value of current where a characteristic intersects the horizontal axis is the short-circuit output current I_{OS}. This is guaranteed to be at least 60 mA for a FAST gate, compared to 40 mA for S-TTL. This parameter is an important indicator of the ability of an output to charge load capacitance. Thus the FAST specifications insure that an output can charge load capacitance faster, or force a higher LOW-to-HIGH voltage step into the dynamic impedance of a long interconnection.

The output HIGH characteristics of a buffer are shown in *Figure 2-14*. These are similar in shape to *Figure 2-13* but at higher levels of current. The output HIGH voltage of a buffer is guaranteed at two different levels of load current. With a 3 mA load, V_{OH} is guaranteed to be at least 2.4 V for both Military and Commercial devices. V_{OH} is also guaranteed to be at least 2.0 V with a 12 mA load for Military or 15 mA load for Commercial devices. In addition, the short-circuit output current of a buffer is guaranteed to be at least 100 mA.

When an output is driving a long interconnection, the initial LOW-to-HIGH transition is somewhat less than the final, quiescent HIGH level because of the loading effect of the line impedance. The full HIGH voltage level is only reached after the reflection from the far end of the line returns to the driver. The initial LOW-to-HIGH voltage step that an output can force into a line is determined by drawing a load line on the graph containing the output HIGH characteristic and noting the voltage value where the load line intersects the characteristic. For example, if a FAST gate is driving a 100 Ω line, a straight line from the lower left origin up to the point 5 V, 50 mA intersects the characteristic curve at about 2.8 V. This indicates that the gate output voltage will rise to 2.8 V initially, and the 2.8 V signal, accompanied by 28 mA of current, will travel to the end of the line. If not terminated, the 28 mA is forced to return to the driver, whereupon it unloads the driver and the output voltage rises to the maximum value. Similarly, a 50 Ω load line drawn on the buffer characteristic shows an intercept voltage of 2.5 V. In both cases, the initial voltage step is great enough to pass through the switching region of any inputs that might be located near the driver end of the line, and thus would not exhibit any exaggerated propagation delay due to the loading effect of the line impedance on the driver output. Thus the FAST output characteristics insure better system performance under adverse loading conditions.

Input Characteristics

The input of a FAST circuit represents a small capacitance, typically 4 to 5 pF, in parallel with an I-V characteristic that exhibits different slopes over different ranges of input voltage. *Figure 2-15* shows the input characteristic of a FAST gate at three temperatures. In the upper right, the flat horizontal portion is the V_{IH} - I_{IH} characteristic. In this region, all of the current from the 10K input resistor (*Figure 2-3*) is flowing into the base of Q1 and the only current flowing in the input diode is the leakage current I_{IH}. When the input voltage decreases to about 1.7 V (+25°C), current starts to flow out of the input diode and the curve shows a knee. At this point some of the current from the 10K resistor is diverted from the base of Q1. When

Fig. 2-14 Output HIGH Characteristics — 'F244

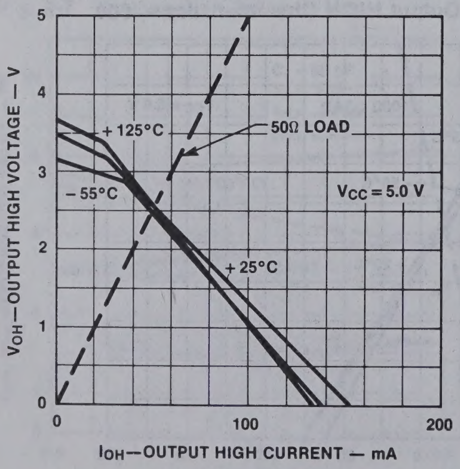
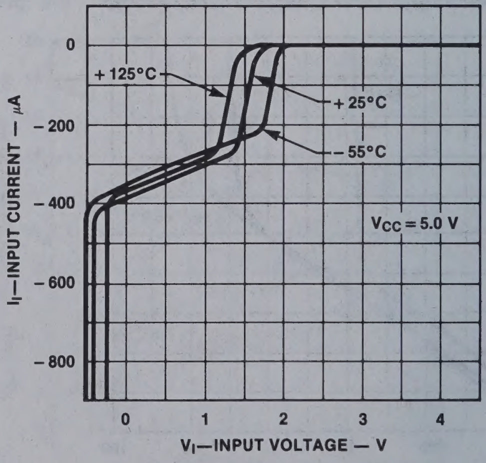


Fig. 2-15 Input Characteristics — 'F00



the input voltage declines to about 1.4 V the curve shows another knee; at this point, substantially all of the current from the 10K resistor flows out of the input diode. The portion of the curve between 1.4 V and 1.7 V input voltage is the active region, essentially corresponding to the FAST transfer function in *Figure 2-5.*

Below 1.4 V input, the characteristic has the slope of the 10K input resistor. When the input voltage declines to about -0.3 V, the Schottky clamping diode starts conducting and the current increases rapidly as the input voltage decreases further.

The input characteristics of a buffer, shown in *Figure 2-16*, differ from those of a gate in two respects. One is the location of the transition region along the horizontal axis. A buffer input has a hysteresis characteristic about 400 mV wide, such that the transition region shifts left or right accordingly as the input voltage transition is HIGH-to-LOW or LOW-to-HIGH, respectively. The curves in *Figure 2-16* apply to the HIGH-to-LOW input voltage transition. The other difference between buffer and gate characteristics is the slope of the curves below the transition region. The input resistor of a buffer is 4 KΩ, and the slope of the characteristic follows this value, rather than the 10 KΩ slope of a gate input.

The characteristics of an input Schottky clamp diode are shown in *Figure 2-17*, for much larger values of current than those of *Figures 2-15* and *2-16*. The purpose of the clamp diode is to limit undershoot at the end of a line following a HIGH-to-LOW signal transition. For example, an output signal change from +3.5 V to +0.5 V into a 100 Ω line propagates to the end of the line, accompanied by a 30 mA current change. If the line is terminated in a high impedance the 3 V signal change doubles, driving the terminal voltage down to -2.5 V. With the clamp diode, however, the negative excursion would be limited to about -0.7 V. The same HIGH-to-LOW signal change on a 50 Ω line would be clamped at about -1.0 V. *Figure 2-18* shows the typical breakdown characteristics for a FAST input.

Fig. 2-17 Input Characteristics — 'F00 or 'F244

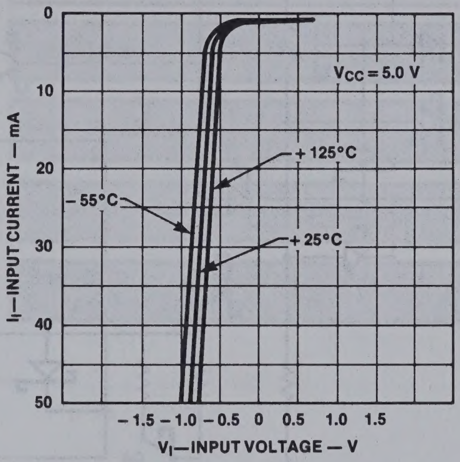


Fig. 2-16 Input Characteristics — 'F244

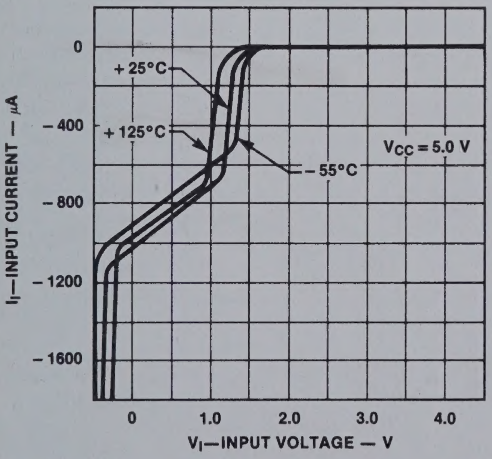
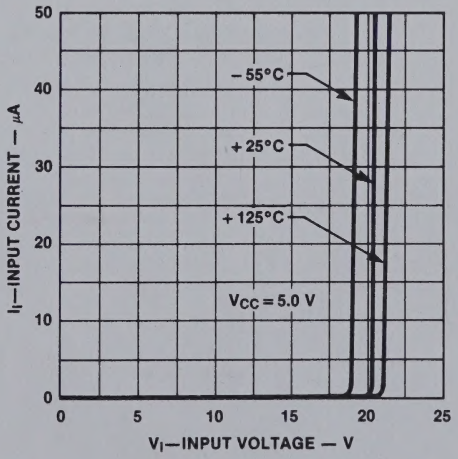


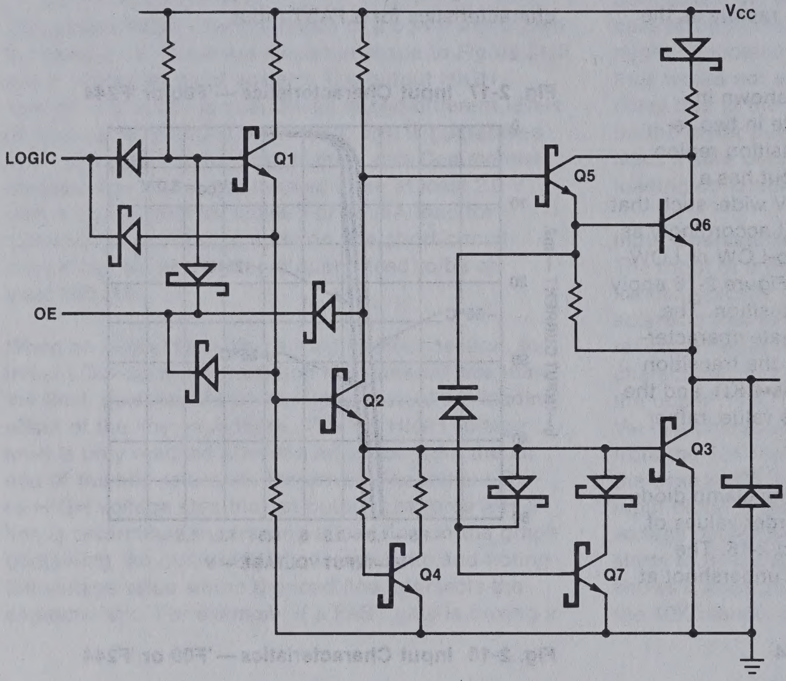
Fig. 2-18 Input Characteristics — 'F00 or 'F244

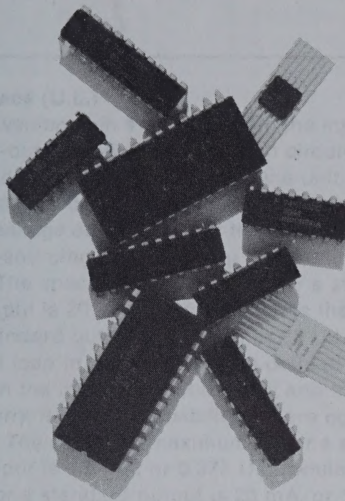


3-State Outputs

A partial schematic of a circuit having a 3-state output is shown in *Figure 2-19*. When the internal Output Enable (OE) signal is HIGH, the circuit operates in the normal fashion to provide HIGH or LOW output drive characteristics. When OE is LOW, however, the bases of Q1, Q2 and Q5 are pulled down. In this condition the output is a high impedance. In this high-Z condition the output leakage is guaranteed not to exceed 50 μA. In the case of a transceiver, each data pin is an input as well as an output and the leakage specification is increased to 70 μA. In the high-Z state, output capacitance averages about 5 pF for a 20 mA output and about 12 pF for a 64 mA output.

Fig. 2-19 Typical 3-State Output Control





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Section 3

Ratings, Specifications and Waveforms

Unit Loads (U.L.)
For convenience in system design, the input loading and fan-out characteristics of each circuit are specified in terms of unit loads. One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current I_{IH} and the output HIGH current-sourcing capability I_{OH} are normalized to 40 μA. The specified maximum I_{IH} for a standard FAST input is 20 μA, or 0.5 U.L., while the I_{OH} rating for a standard output is 1.0 mA, or 25 U.L. Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current I_{IL} and the output LOW current-sinking capability I_{OL} are normalized to 1.6 mA. The specified maximum I_{IL} for a standard FAST input is 0.6 mA, or 0.375 U.L., while the I_{OL} rating for a standard output is 20 mA, or 12.5 U.L. On the data sheets, the input and output load factors are listed in the Input Loading/Fan-Out table. The table from the 54F/74F04 Hex Inverter is reproduced below.

In the right-hand column the input HIGH/LOW load factors are 0.5/0.375, with the first number representing I_{IH} and the second representing I_{IL}. For testing or procurement purposes, these load factors can easily be translated to actual test limits by multiplying them by 40 μA and 1.6 mA, respectively. The second set of numbers represents the rated output HIGH/LOW load currents I_{OH} and I_{OL}, respectively. The indicated HIGH/LOW drive factors of 25/12.5 translate to 1.0 mA and 20 mA by multiplying them by 40 μA and 1.6 mA, respectively.

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

Absolute Maximum Ratings[1]
(beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage[2]	-0.5 V to +7.0 V
Input Current[2]	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State:	
Standard Output	-0.5 V to V_{CC} Value
3-State Output (with V_{CC} = 0 V)	-0.5 V to +5.5 V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL}

Recommended Operating Conditions[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

1. Unless otherwise restricted or extended by detail specifications.
2. Either input voltage or current limit sufficient to protect inputs.

54F/74F Family DC Characteristics[1]

Symbol	Parameter		Limits[2] Min	Typ[3]	Max	Units	V_{CC}[4]	Conditions[2]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	Std[6] Mil	2.5	3.4		V	Min	$I_{OH} = 40$ µA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std[6] Com	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	$I_{OL} = 1.6$ mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	µA	Max	$I_{IH} = 40$ µA Multiplied by Input HIGH U.L. Shown on Data Sheet; $V_{IN} = 2.7$ V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				100	µA	Max	$V_{IN} = 7.0$ V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	$I_{IL} = -1.6$ mA Multiplied by Input LOW U.L. Shown on Data Sheet; $V_{IN} = 0.5$ V
		0.75 U.L.			-1.2			
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				50	µA	Max	$V_{OUT} = 2.4$ V
I_{OZL}	3-State Output OFF Current LOW				-50	µA	Max	$V_{OUT} = 0.5$ V
I_{OS}[5]	Output Short-Circuit Current	Standard[6]/ 3-State	-60		-150	mA	Max	$V_{OUT} = 0$ V
		Buffers/ Line Dvrs	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0$ V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

AC Loading and Waveforms

Figure 3-1 shows the ac loading circuit used in characterizing and specifying propagation delays of all FAST devices, unless otherwise specified in the data sheet of a specific device. The use of this load, which differs somewhat from previous practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the 1980 edition of the FAST data book, the +25°C propagation delays were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance, and implied the use of high-impedance, high-frequency scope probes. Changing to 50 pF of capacitance allows more leeway in stray capacitance and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay figures. The net effect of the change in ac load is to increase the observed propagation delay by an average of about 1 ns.

The 500 Ω resistor to ground, in *Figure 3-1*, acts as a ballast, to slightly load the totem-pole pull-up and limit the quiescent HIGH-state voltage to about +3.5 V. Otherwise, an output would rise quickly to about +3.5 V but then continue to rise very slowly on up to about +4.4 V. On the subsequent HIGH-to-LOW transition the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps more importantly, the 500 Ω resistor to ground can be a high frequency passive probe for a sampling scope, which costs much less than the equivalent high-impedance probe. Alternatively, the 500 Ω load to ground can simply be a 450 Ω resistor feeding into a 50 Ω coaxial cable leading to a sampling scope input connector, with the internal 50 Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 Ω termination for the pulse generator that supplies the input signal.

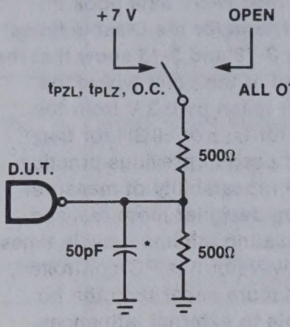
Also shown in *Figure 3-1* is a second 500 Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-state output. With the switch closed, the pair of 500 Ω resistors and the +7.0 V supply establish a quiescent HIGH level of +3.5 V, which correlates with the HIGH level discussed in the preceding paragraph.

Another change from the 1980 FAST data book involves the measurement criteria for the Disable times of 3-state outputs. *Figures 3-12* and *3-13* show that the Disable times are measured at the point where the output voltage has risen or fallen by 0.3 V from the quiescent level (i.e., LOW for t_{PLZ} or HIGH for t_{PHZ}), compared to a ΔV of 0.5 V used in previous practice. This change enhances the repeatability of measurements and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the rising or falling waveform is RC-controlled, the first 0.3 V of change is more linear than the first 0.5 V and is less susceptible to external influences. More importantly, perhaps, from the system designer's point of view, a ΔV of 0.3 V is adequate to ensure that a device output has turned OFF; measuring to a ΔV of 0.5 V merely exaggerates the apparent Disable time and thus penalizes system performance, since the designer must use the Enable and Disable times to devise worst-case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Good high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible, to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used, for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5 ns and signal swing of 0 V to +3.0 V. A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Precautions should be taken to prevent damage to devices by electrostatic charge. Static charge tends to accumulate on insulated surfaces, such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. In extremely adverse environments, it may be necessary for individuals to wear a grounded wrist strap when handling devices.

Fig. 3-1 Test Load


+7 V
OPEN
tPZL, tPLZ, O.C.
ALL OTHER
500Ω
D.U.T.
50pF
*
500Ω

*INCLUDES JIG AND PROBE CAPACITANCE

Fig. 3-2 Propagation Delays from Up/Down Control

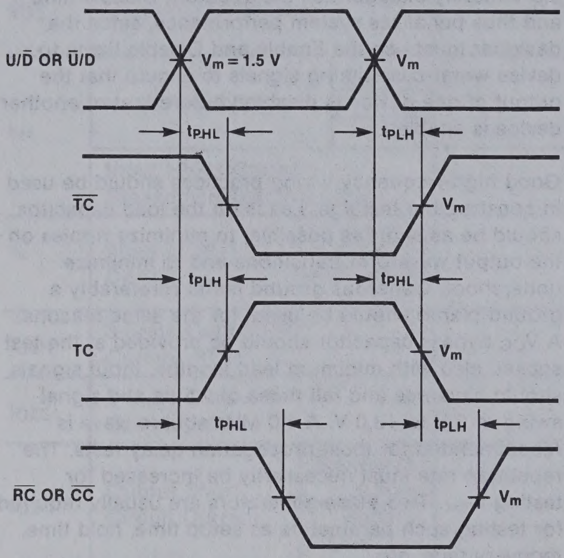
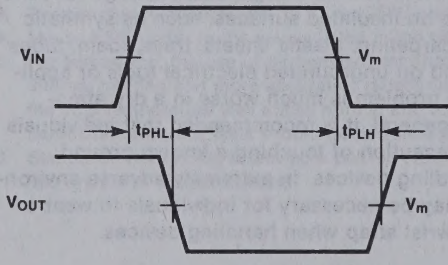
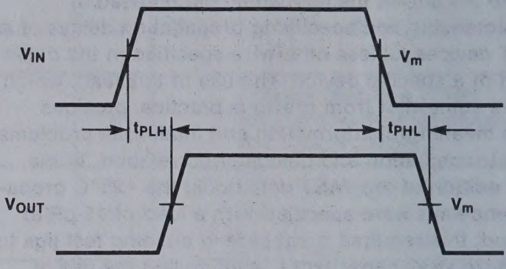

U/D̄ OR Ū/D
Vm = 1.5 V
Vm
tPHL
tPLH
T̄C̄
Vm
tPLH
tPHL
TC
Vm
tPHL
tPLH
R̄C̄ OR C̄C̄
Vm

Fig. 3-3 Waveform for Inverting Functions


VIN
Vm
tPHL
tPLH
VOUT
Vm

Vm = 1.5 V

Fig. 3-4 Waveform for Non-inverting Functions


VIN
Vm
tPLH
tPHL
VOUT
Vm

Vm = 1.5 V

Fig. 3-5 Setup and Hold Times, Rising-edge Clock

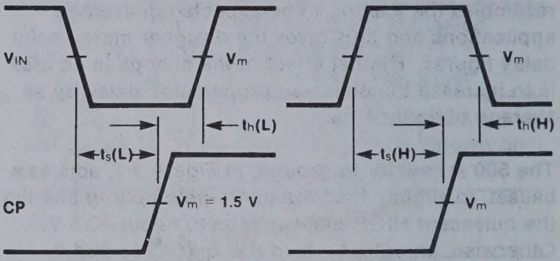

VIN
Vm
Vm
th(L)
th(H)
ts(L)
ts(H)
CP
Vm = 1.5 V
Vm

Fig. 3-6 Setup and Hold Times, Falling-edge Clock

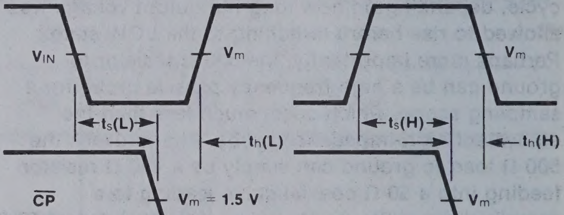

VIN
Vm
Vm
ts(L)
th(L)
ts(H)
th(H)
C̄P̄
Vm = 1.5 V
Vm

Fig. 3-7 Propagation Delays from Rising-edge Clock or Enable

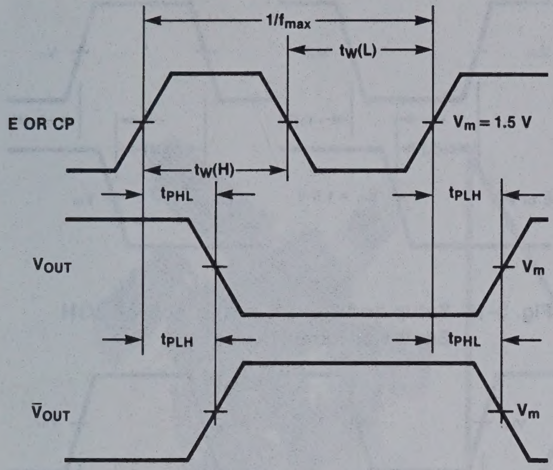

1/f_{max}
$t_W(L)$
E OR CP
$V_m = 1.5$ V
$t_W(H)$
t_{PHL}
t_{PLH}
V_{OUT}
V_m
t_{PLH}
t_{PHL}
$\overline{V}_{OUT}$
V_m

Fig. 3-8 Propagation Delays from Falling-edge Clock or Enable

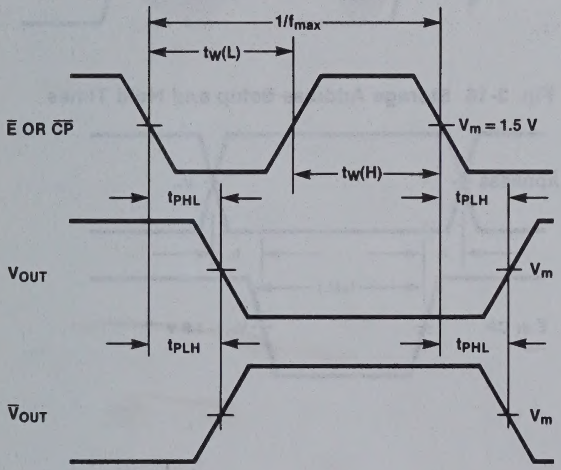

1/f_{max}
$t_W(L)$
$\overline{E}$ OR $\overline{CP}$
$V_m = 1.5$ V
$t_W(H)$
t_{PHL}
t_{PLH}
V_{OUT}
V_m
t_{PLH}
t_{PHL}
$\overline{V}_{OUT}$
V_m

Fig. 3-9 Propagation Delays from Set and Clear (or Reset)

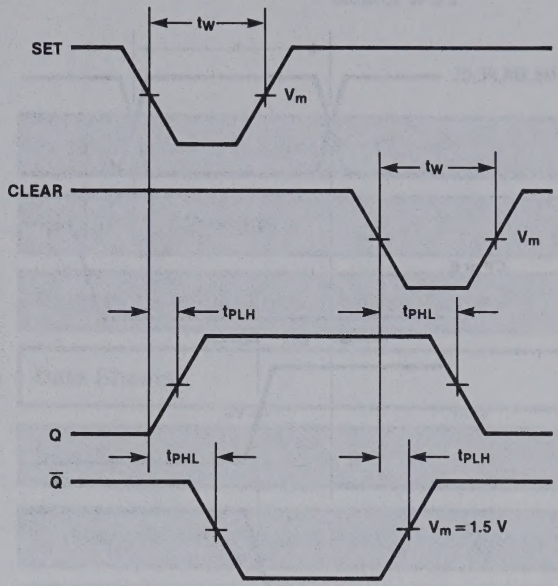

t_W
SET
V_m
t_W
CLEAR
V_m
t_{PLH}
t_{PHL}
Q
t_{PHL}
t_{PLH}
$\overline{Q}$
$V_m = 1.5$ V

Fig. 3-10 Whether Response Is Inverting or Non-Inverting Depends on Specific Truth Table Conditions

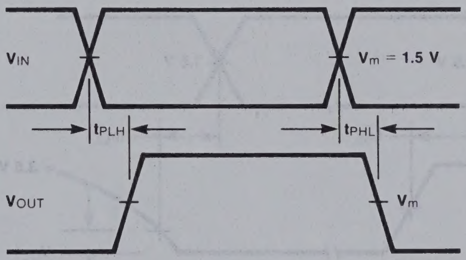

V_{IN}
$V_m = 1.5$ V
t_{PLH}
t_{PHL}
V_{OUT}
V_m

Fig. 3-11 Asynchronous Set, Reset, Parallel Load or Clear, Active Rising-edge Clock or Active-LOW Enable

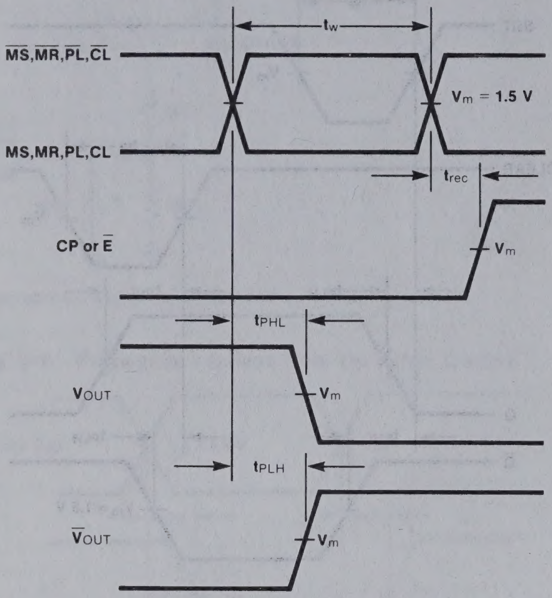

t_w
$\overline{\text{MS}},\overline{\text{MR}},\overline{\text{PL}},\overline{\text{CL}}$
$V_m = 1.5$ V
MS,MR,PL,CL
t_{rec}
CP or $\overline{\text{E}}$
V_m
t_{PHL}
V_{OUT}
V_m
t_{PLH}
$\overline{V}_{OUT}$
V_m

Fig. 3-12 3-State Output LOW Enable and Disable Times

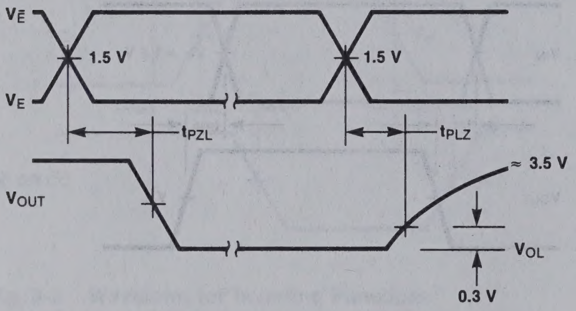

$V_{\overline{E}}$
1.5 V
1.5 V
V_E
t_{PZL}
t_{PLZ}
≈ 3.5 V
V_{OUT}
V_{OL}
0.3 V

Fig. 3-13 3-State Output HIGH Enable and Disable Times

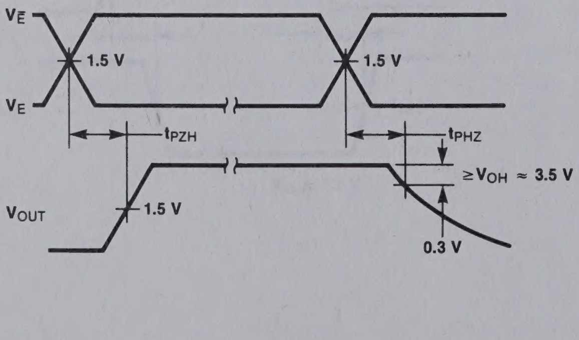

$V_{\overline{E}}$
1.5 V
1.5 V
V_E
t_{PZH}
t_{PHZ}
$\geq V_{OH} \approx 3.5$ V
V_{OUT}
1.5 V
0.3 V

Fig. 3-14 Setup and Hold Times to Active-LOW Enable or Parallel Load

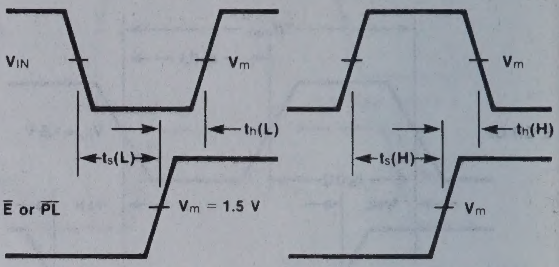

V_{IN}
V_m
V_m
$t_h(L)$
$t_h(H)$
$t_s(L)$
$t_s(H)$
$\overline{\text{E}}$ or $\overline{\text{PL}}$
$V_m = 1.5$ V
V_m

Fig. 3-15 Setup and Hold Times to Active-HIGH Enable or Parallel Load

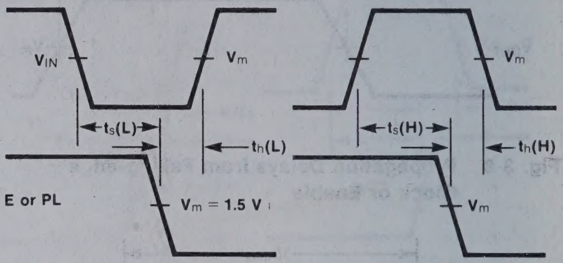
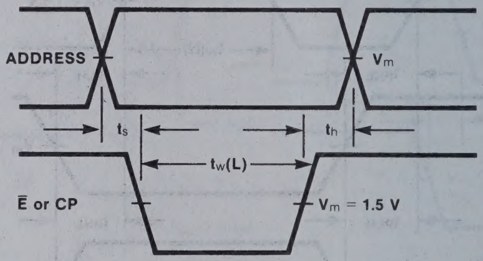
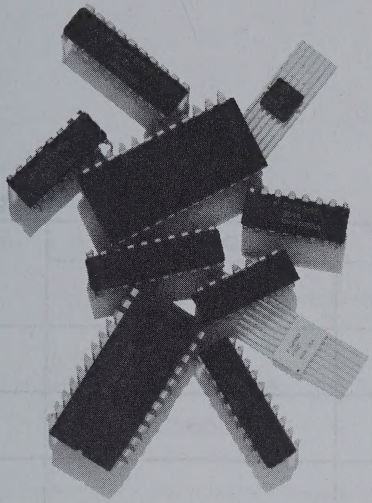

V_{IN}
V_m
V_m
$t_s(L)$
$t_h(L)$
$t_s(H)$
$t_h(H)$
E or PL
$V_m = 1.5$ V
V_m

Fig. 3-16 Storage Address Setup and Hold Times


ADDRESS
V_m
t_s
t_h
$t_w(L)$
$\overline{\text{E}}$ or CP
$V_m = 1.5$ V



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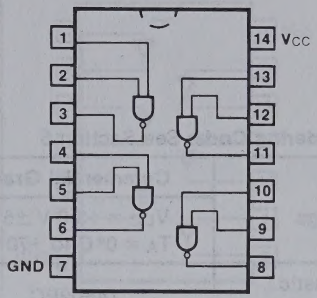
54F/74F00

Quad 2-Input NAND Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F00PC		9A
Ceramic DIP (D)	74F00DC	54F00DM	6A
Flatpak (F)		54F00FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current		1.9 6.8	2.8 10.2	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

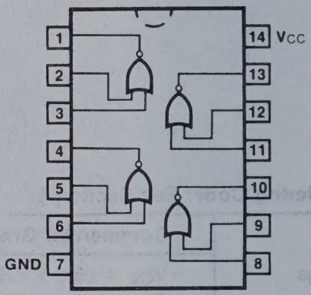
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	2.4 2.0	6.0 5.3	ns	3-1 3-3

54F/74F02

Quad 2-Input NOR Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	Pkg Type
Plastic DIP (P)	74F02PC		9A
Ceramic DIP (D)	74F02DC	54F02DM	6A
Flatpak (F)		54F02FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current		3.7 8.7	5.6 13	mA	V_{IN} = Gnd *	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

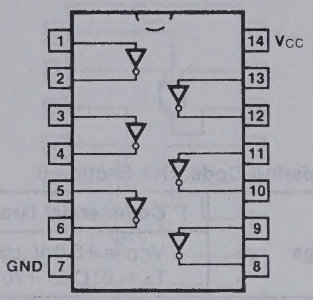
Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.5 2.0	4.4 3.2	5.5 4.3	2.5 1.5	7.5 6.5	2.5 2.0	6.5 5.3	ns	3-1 3-3

*Measured with one input HIGH, one input LOW for each gate.

54F/74F04

Hex Inverter

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	Pkg Type
Plastic DIP (P)	74F04PC		9A
Ceramic DIP (D)	74F04DC	54F04DM	6A
Flatpak (F)		54F04FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		2.8	4.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			10.2	15.3		V_{IN} = Open	

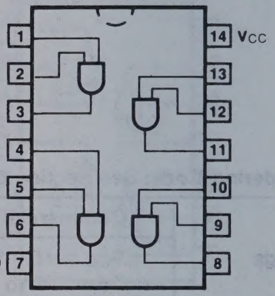
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		2.0	3.2	4.3	1.5	6.5	2.0	5.3		3-3

54F/74F08

Quad 2-Input AND Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F08PC		9A
Ceramic DIP (D)	74F08DC	54F08DM	6A
Flatpak (F)		54F08FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		5.5	8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			8.6	12.9		V_{IN} = Gnd	

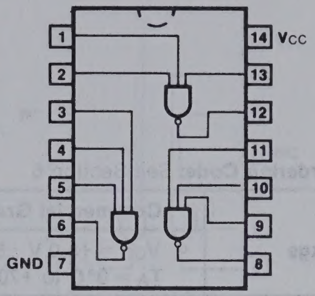
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	3-1
t_{PHL}		2.5	4.0	5.3	2.0	7.5	2.5	6.3		3-4

54F/74F10

Triple 3-Input NAND Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F10PC		9A
Ceramic DIP (D)	74F10DC	54F10DM	6A
Flatpak (F)		54F10FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		1.4	2.1	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			5.1	7.7		V_{IN} = Open	

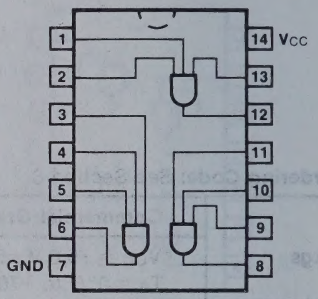
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		2.0	3.2	4.3	1.5	6.5	2.0	5.3		3-3

54F/74F11

Triple 3-Input AND Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F11PC		9A
Ceramic DIP (D)	74F11DC	54F11DM	6A
Flatpak (F)		54F11FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		4.1	6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			6.5	9.7		V_{IN} = Gnd	

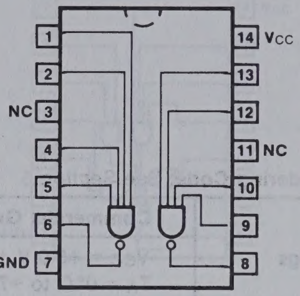
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	3-1
t_{PHL}		2.5	4.1	5.5	2.0	7.5	2.5	6.5		3-4

54F/74F20

Dual 4-Input NAND Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F20PC		9A
Ceramic DIP (D)	74F20DC	54F20DM	6A
Flatpak (F)		54F20FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
I_{CCH} I_{CCL}	Power Supply Current		0.9 3.4	1.4 5.1	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

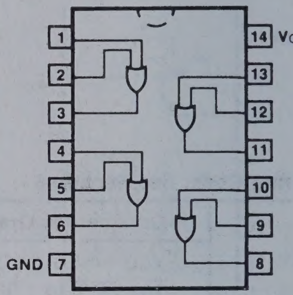
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	2.4 2.0	6.0 5.3	ns	3-1 3-3

54F/74F32

Quad 2-Input OR Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F32PC		9A
Ceramic DIP (D)	74F32DC	54F32DM	6A
Flatpak (F)		54F32FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		6.1	9.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			10.3	15.5		V_{IN} = Gnd	

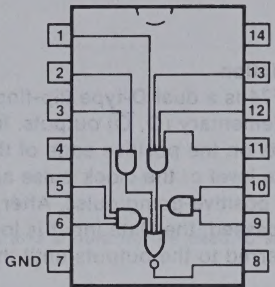
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.2	5.6	3.0	7.5	3.0	6.6	ns	3-1
t_{PHL}		3.0	4.0	5.3	2.5	7.5	3.0	6.3		3-4

54F/74F64

4-2-3-2-Input AND OR-Invert Gate

Connection Diagram



Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	Pkg Type
Plastic DIP (P)	74F64PC		9A
Ceramic DIP (P)	74F64DC	54F64DM	6A
Flatpak (F)		54F64FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		1.9	2.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			3.1	4.7		*	

AC Characteristics: See Section 3 for waveforms and load configurations

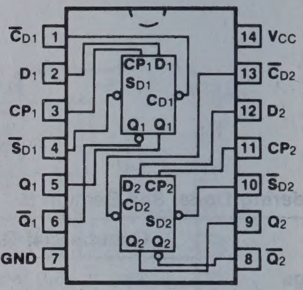
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.6	6.0	2.5	8.0	2.5	7.0	ns	3-1
t_{PHL}		2.0	3.2	4.5	1.5	6.5	2.0	5.5		3-3

*I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

54F/74F74

Dual D-Type Positive Edge-Triggered Flip-Flop

Connection Diagram


$\overline{C}_{D1}$ 1
D1 2
CP1 3
$\overline{S}_{D1}$ 4
Q1 5
$\overline{Q}_1$ 6
GND 7
14 VCC
13 $\overline{C}_{D2}$
12 D2
11 CP2
10 $\overline{S}_{D2}$
9 Q2
8 $\overline{Q}_2$
CP1 D1
SD1
CD1
Q1 Q1
D2 CP2
CD2
SD2
Q2 Q2

Description

The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

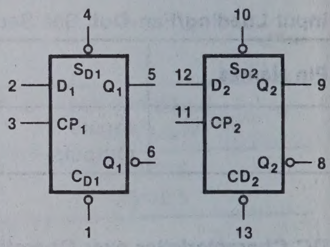
Truth Table
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

Logic Symbol


4
10
SD1
D1
Q1
CP1
Q1
CD1
2
3
5
6
1
SD2
D2
Q2
CP2
Q2
CD2
12
11
9
8
13

VCC = Pin 14
GND = Pin 7

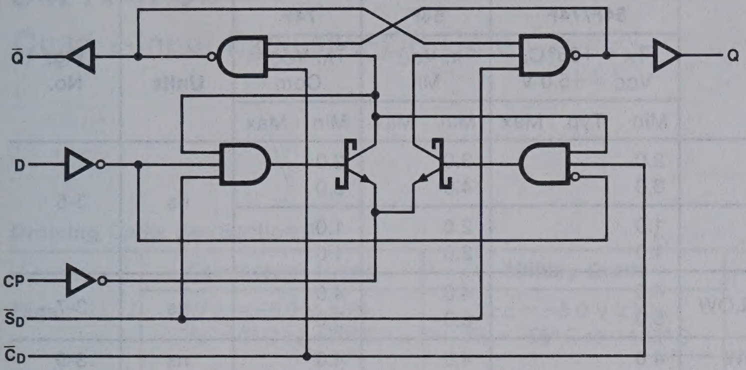
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	VCC = +5.0 V ±5%, T_A = 0° C to +70° C	VCC = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F74PC		9A
Ceramic DIP (D)	74F74DC	54F74DM	6A
Flatpak (F)		54F74FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
D1, D2	Data Inputs	0.5/0.375
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q1, $\overline{Q}_1$, Q2, $\overline{Q}_2$	Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		10.5	16	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		100		100		MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	8.5 10.5	3.8 4.4	7.8 9.2	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	3.2 3.5	7.1 10.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW D_n to CP_n	2.0			3.0		2.0		ns	3-5
t_s (L)		3.0			4.0		3.0			
t_h (H)	Hold Time, HIGH or LOW D_n to CP_n	1.0			2.0		1.0			
t_h (L)		1.0			2.0		1.0			
t_w (H)	CP_n Pulse Width, HIGH or LOW	4.0			4.0		4.0		ns	3-7
t_w (L)		5.0			6.0		5.0			
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns	3-9
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			3.0		2.0		ns	3-11

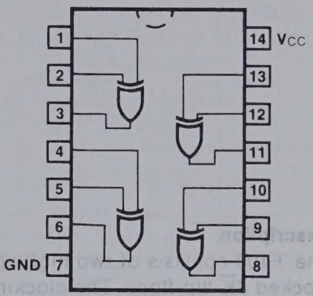
54F/74F86

Quad 2-Input Exclusive-OR Gate

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = −55° C to +125° C	
Plastic DIP (P)	74F86PC		9A
Ceramic DIP (D)	74F86DC	54F86DM	6A
Flatpak (F)		54F86FM	3I

Connection Diagram



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54/74LS Min	54/74LS Typ	54/74LS Max	Units	Conditions	
I_{CC}	Power Supply Current		15	23	mA	Inputs LOW	V_{CC} = Max
			18	28		Inputs HIGH	

AC Characteristics: See Section 3 for waveforms and load configurations

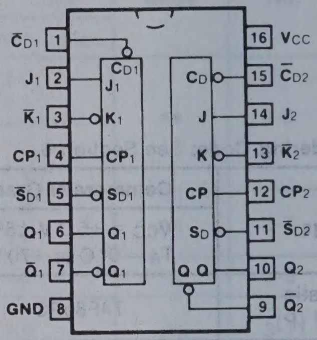
Symbol	Parameter	54F/74F T_A = +25° C V_{CC} = +5.0 V C_L = 50 pF			54/F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay (Other Input LOW)	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	7.0 7.0	3.0 3.0	6.5 6.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay (Other Input HIGH)	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.5 8.0	3.5 3.0	8.0 7.5	ns	3-1 3-3

▨ Test limits in screened columns are preliminary.

54F/74F109

Dual J$\overline{\text{K}}$ Positive Edge-Triggered Flip-Flop

Connection Diagram


$\overline{\text{C}}_{D1}$
1
J1
2
$\overline{\text{K}}_1$
3
CP1
4
$\overline{\text{S}}_{D1}$
5
Q1
6
$\overline{\text{Q}}_1$
7
GND
8
16
VCC
15
$\overline{\text{C}}_{D2}$
14
J2
13
$\overline{\text{K}}_2$
12
CP2
11
$\overline{\text{S}}_{D2}$
10
Q2
9
$\overline{\text{Q}}_2$
CD1
J1
K1
CP1
SD1
Q1
Q1
CD
J
K
CP
SD
Q Q

Description

The 'F109 consists of two high-speed, completely independent transition clocked J$\overline{\text{K}}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{\text{K}}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{\text{K}}$ inputs together.

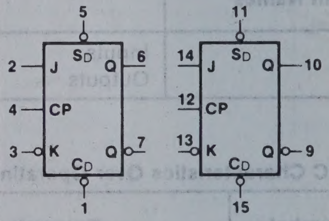
Truth Table

INPUTS		OUTPUTS	
@ t_n		@ t_{n+1}	
J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:
LOW input to $\overline{\text{S}}_D$ sets Q to HIGH level
LOW input to $\overline{\text{C}}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{\text{C}}_D$ and $\overline{\text{S}}_D$ makes both Q and $\overline{\text{Q}}$ HIGH

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Symbol


5
11
2
J
SD
Q
6
14
J
SD
Q
10
4
CP
12
CP
3
K
Q
7
13
K
Q
9
CD
CD
1
15

VCC = Pin 16
GND = Pin 8

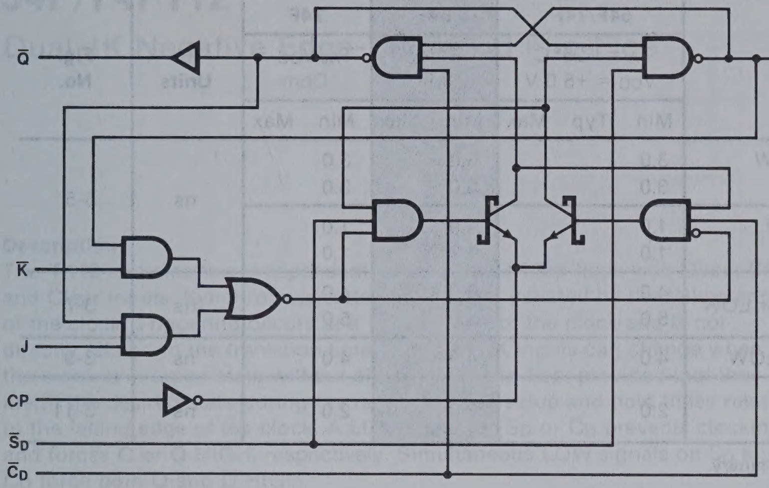
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F109PC		9B
Ceramic DIP (D)	74F109DC	54F109DM	6B
Flatpak (F)		54F109FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
J1, J2, $\overline{\text{K}}_1$, $\overline{\text{K}}_2$	Data Inputs	0.5/0.375
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{\text{C}}_{D1}$, $\overline{\text{C}}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{\text{S}}_{D1}$, $\overline{\text{S}}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q1, Q2, $\overline{\text{Q}}_1$, $\overline{\text{Q}}_2$	Outputs	25/12.5

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		11.7	17	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	90	125		90		90		MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n to $\overline{Q}_n$	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	3.8 4.4	8.0 9.2	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	9.0 11.5	3.2 3.5	8.0 10.5	ns	3-1 3-9

▩ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

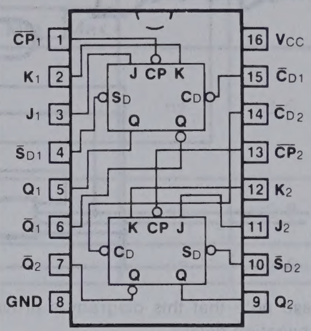
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	1.0 1.0			1.0 1.0		1.0 1.0			
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns	3-7
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns	3-9
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			2.0		2.0		ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F112

Dual JK Negative Edge-Triggered Flip-Flop

Connection Diagram


$\overline{CP}_1$ 1
K1 2
J1 3
$\overline{S}_{D1}$ 4
Q1 5
$\overline{Q}_1$ 6
$\overline{Q}_2$ 7
GND 8
16 VCC
15 $\overline{C}_{D1}$
14 $\overline{C}_{D2}$
13 $\overline{CP}_2$
12 K2
11 J2
10 $\overline{S}_{D2}$
9 Q2
J CP K
SD
CD
Q
Q
K CP J
CD
SD
Q
Q

Description

The 'F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Truth Table

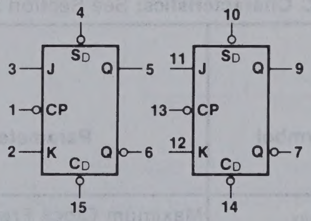
INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:

LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Symbol


4
10
SD
SD
3
J
Q
5
11
J
Q
9
1
CP
13
CP
2
K
Q
6
12
K
Q
7
CD
CD
15
14

V_{CC} = Pin 16
GND = Pin 8

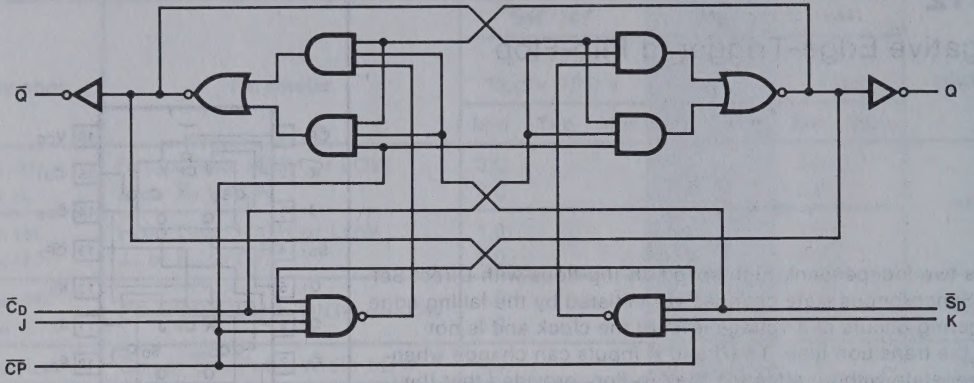
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	Pkg Type
Plastic DIP (P)	74F112PC		9B
Ceramic DIP (D)	74F112DC	54F112DM	6B
Flatpak (F)		54F112FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0.5/1.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.875
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

		54F/74F			54F		74F			
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
Symbol	Parameter	Min	Typ	Max	Min	Max	Min	Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	100	125						MHz	3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	3.3 3.3	5.5 5.5	7.7 7.7					ns	3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 3.3	5.0 5.5	7.0 7.7					ns	3-1, 3-9

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

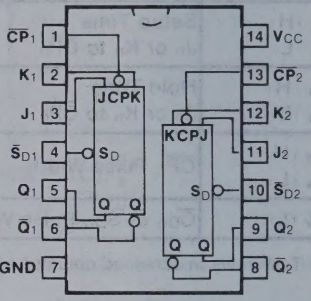
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	3.0 3.0							ns	3-6
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0								
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	5.0 5.0							ns	3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	5.0							ns	3-9

▨ Test limits in screened columns are preliminary.

54F/74F113

Dual JK Edge-Triggered Flip-Flop

Connection Diagram


$\overline{CP}_1$ 1
K_1 2
J_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{CP}_2$
12 K_2
11 J_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
JCPK
KCPJ
S_D
Q Q

Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Truth Table

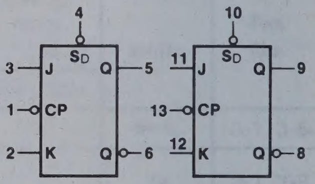
INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Input:

LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Symbol


4
10
S_D
J
Q
CP
K
3
5
1
2
6
11
9
13
12
8

V_{CC} = Pin 14
GND = Pin 7

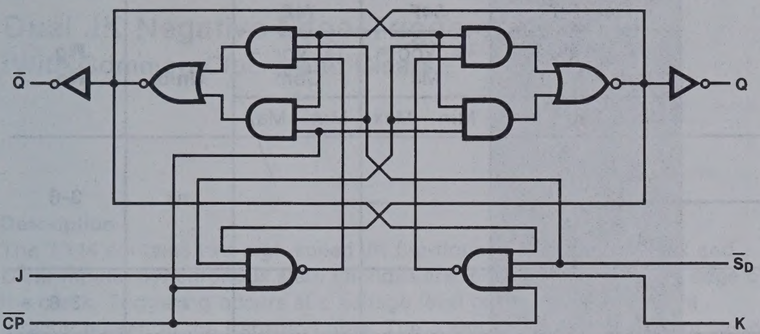
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F113PC		9A
Ceramic DIP (D)	74F113DC	54F113DM	6A
Flatpak (F)		54F113FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0.5/1.50
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125						MHz	3-1, 3-8
t_{PLH}	Propagation Delay	3.3	5.5	7.7					ns	3-1
t_{PHL}	$\overline{CP}_n$ to Q_n or $\overline{Q}_n$	3.3	5.5	7.7						3-8
t_{PLH}	Propagation Delay	3.0	5.0	7.0					ns	3-1
t_{PHL}	$\overline{S}_{DN}$ to Q_n or $\overline{Q}_n$	3.3	5.5	7.7						3-9

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

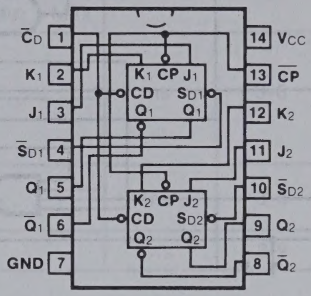
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	3.0 3.0							ns	3-6
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0								
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	5.0 5.0							ns	3-8
t_w (L)	$\overline{S}_{DN}$ Pulse Width LOW	5.0							ns	3-9

▨ Test limits in screened columns are preliminary.

54F/74F114

Dual JK Negative Edge-Triggered Flip-Flop
(With Common Clocks and Clears)

Connection Diagram


$\overline{C}_D$ 1
K_1 2
J_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{CP}$
12 K_2
11 J_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
K_1 CP J_1
CD S_{D1}
Q_1 $\overline{Q}_1$
K_2 CP J_2
CD S_{D2}
Q_2 $\overline{Q}_2$

Description

The 'F114 contains two high-speed JK flip-flops with common clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

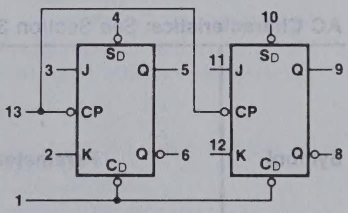
Truth Table

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

Logic Symbol


4
10
S_D
S_D
3
J
Q
5
11
J
Q
9
13
CP
CP
2
K
C_D
Q
6
12
K
C_D
Q
8
1

V_{CC} = Pin 14
GND = Pin 7

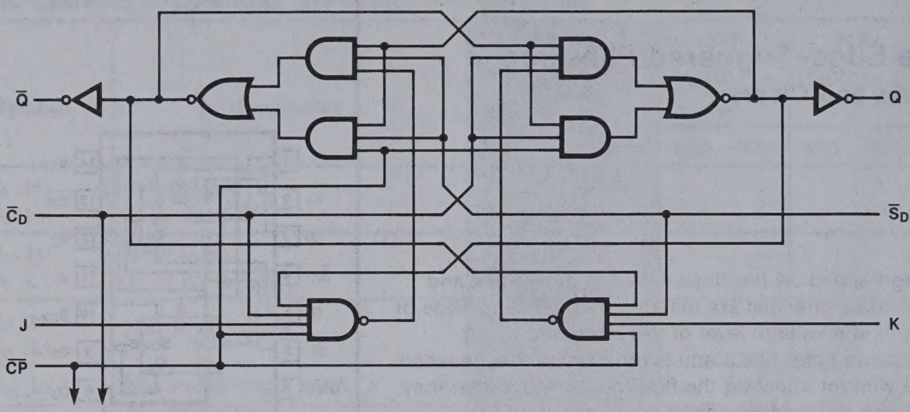
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F114PC		9A
Ceramic DIP (D)	74F114DC	54F114DM	6A
Flatpak (F)		54F114FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/1.50
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/1.875
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF Min	 Typ	 Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	 Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	 Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	100	125						MHz	3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	3.3 3.3	5.5 5.5	7.7 7.7					ns	3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 3.3	5.0 5.5	7.0 7.7					ns	3-1, 3-9

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time	3.0							ns	3-6
t_s (L)	J_n or K_n to $\overline{CP}$	3.0								
t_h (H)	Hold Time	0								
t_h (L)	J_n or K_n to $\overline{CP}$	0								
t_w (H)	$\overline{CP}$ Pulse Width	5.0							ns	3-8
t_w (L)		5.0								
t_w	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width	5.0							ns	3-9

▨ Test limits in screened columns are preliminary.

54F/74F138

1-of-8 Decoder/Demultiplexer

Description

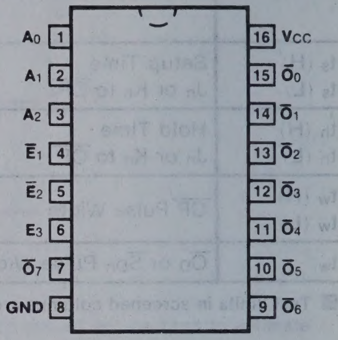
The 'F138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'F138 devices or a 1-of-32 decoder using four 'F138 devices and one inverter.

- **FAST Process for High Speed**
- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active-LOW Mutually Exclusive Outputs**

Ordering Code: See Section 6

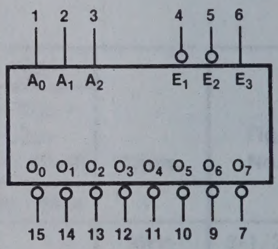
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F138PC		9B
Ceramic DIP (D)	74F138DC	54F138DM	6B
Flatpak (F)		54F138FM	4L

Connection Diagram



A0 1
A1 2
A2 3
E1 4
E2 5
E3 6
O7 7
GND 8
16 VCC
15 O0
14 O1
13 O2
12 O3
11 O4
10 O5
9 O6

Logic Symbol



1
2
3
4
5
6
A0
A1
A2
E1
E2
E3
O0
O1
O2
O3
O4
O5
O6
O7
15
14
13
12
11
10
9
7

V_{CC} = Pin 16
GND = Pin 8

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	0.5/0.375
$\overline{E}_1, \overline{E}_2$	Enable Inputs (Active LOW)	0.5/0.375
E_3	Enable Input (Active HIGH)	0.5/0.375
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5

Functional Description

The ’F138 high-speed 1-of-8 decoder/multiplexer fabricated with the FAST process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The ’F138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four ’F138 devices and one inverter (See *Figure a*). The ’F138 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

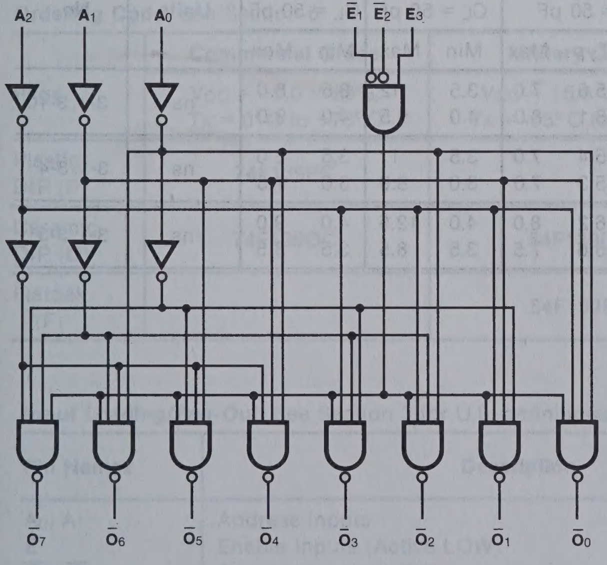
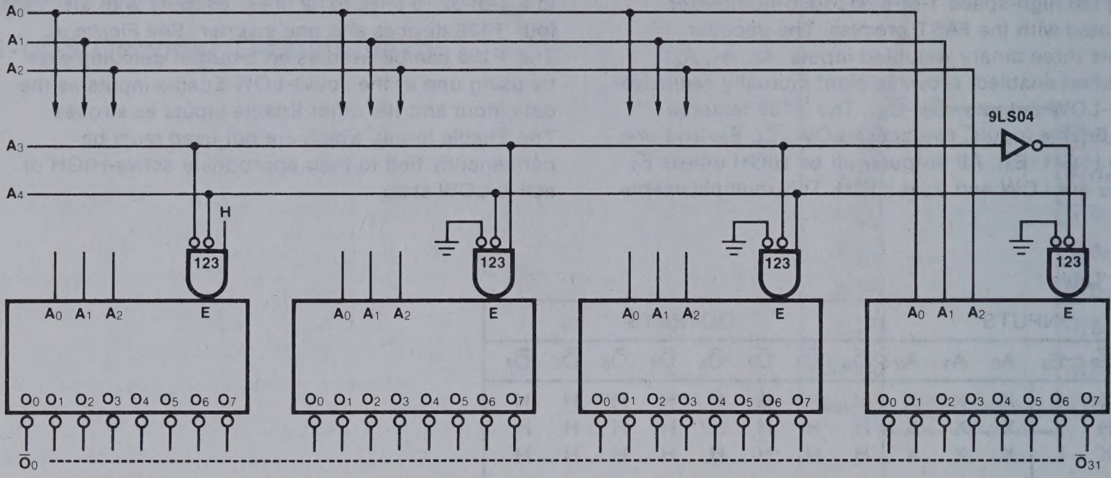


Fig. a Expansion to 1-of-32 Decoding



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13	20	mA	V_{CC} = Max

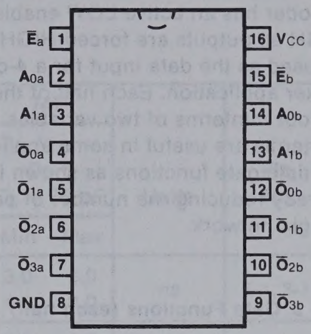
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.5	5.6	7.0	3.5	12	3.5	8.0	ns	3-1, 3-10
t_{PHL}		4.0	6.1	8.0	4.0	9.5	4.0	9.0		
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.5	5.4	7.0	3.5	11	3.5	8.0	ns	3-1, 3-4
t_{PHL}		3.0	5.3	7.0	3.0	8.0	3.0	7.5		
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	4.0	6.2	8.0	4.0	12.5	4.0	9.0	ns	3-1, 3-3
t_{PHL}		3.5	5.6	7.5	3.5	8.5	3.5	8.5		

54F/74F139

Dual 1-of-4 Decoder

Connection Diagram

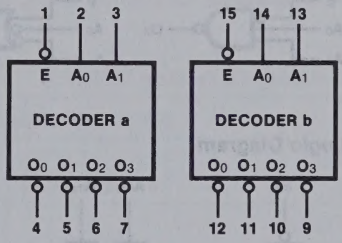

$\overline{E}_a$ 1
A_{0a} 2
A_{1a} 3
$\overline{O}_{0a}$ 4
$\overline{O}_{1a}$ 5
$\overline{O}_{2a}$ 6
$\overline{O}_{3a}$ 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 A_{0b}
13 A_{1b}
12 $\overline{O}_{0b}$
11 $\overline{O}_{1b}$
10 $\overline{O}_{2b}$
9 $\overline{O}_{3b}$

Description

The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'F139 can be used as a function generator providing all four minterms of two variables.

- **Multifunction Capability**
- **Two Completely Independent 1-of-4 Decoders**
- **Active LOW Mutually Exclusive Outputs**

Logic Symbol


1
2
3
E
A_0
A_1
DECODER a
O_0
O_1
O_2
O_3
4
5
6
7
15
14
13
E
A_0
A_1
DECODER b
O_0
O_1
O_2
O_3
12
11
10
9

V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F139PC		9B
Ceramic DIP (D)	74F139DC	54F139DM	6B
Flatpak (F)		54F139FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	0.5/0.375
$\overline{E}$	Enable Inputs (Active LOW)	0.5/0.375
$\overline{O}_0$ - $\overline{O}_3$	Outputs (Active LOW)	25/12.5

Functional Description

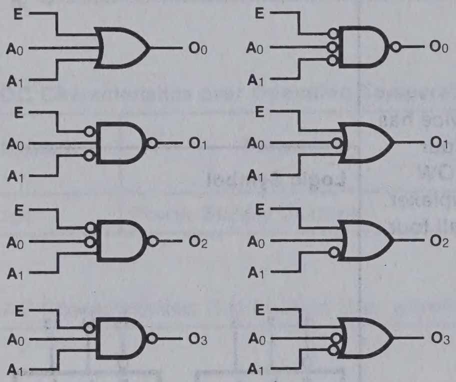
The 'F139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighed inputs (A_0, A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$ - $\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'F139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure a*, and thereby reducing the number of packages required in a logic network.

Truth Table

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

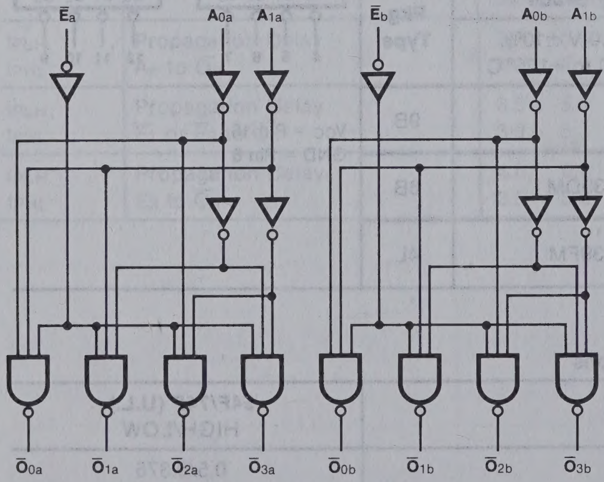
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Fig. a Gate Functions (each half)



E
A0
A1
O0
E
A0
A1
O0
E
A0
A1
O1
E
A0
A1
O1
E
A0
A1
O2
E
A0
A1
O2
E
A0
A1
O3
E
A0
A1
O3

Logic Diagram



Ēa
A0a
A1a
Ēb
A0b
A1b
Ō0a
Ō1a
Ō2a
Ō3a
Ō0b
Ō1b
Ō2b
Ō3b

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13	20	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	3.5 4.0	5.3 6.1	7.0 8.0	2.5 3.5	9.5 9.5	3.0 4.0	8.0 9.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	3.5 3.0	5.4 4.7	7.0 6.5	3.0 2.5	9.0 8.0	3.5 3.0	8.0 7.5	ns	3-1, 3-4

54F/74F148

8-Line to 3-Line Priority Encoder

Description

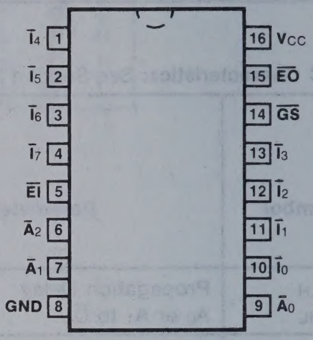
The 'F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

- **Encodes Eight Data Lines in Priority**
- **Provides 3-Bit Binary Priority Code**
- **Input Enable Capability**
- **Signals When Data Present on Any Input**
- **Cascadable for Priority Encoding of n Bits**

Ordering Code: See Section 6

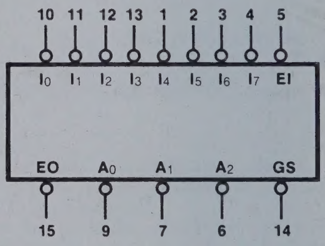
Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F148PC		9B
Ceramic DIP (D)	74F148DC	54F148DM	6B
Flatpak (F)		54F148FM	4L

Connection Diagram



$\overline{I}_4$ 1
$\overline{I}_5$ 2
$\overline{I}_6$ 3
$\overline{I}_7$ 4
$\overline{EI}$ 5
$\overline{A}_2$ 6
$\overline{A}_1$ 7
GND 8
16 V_{CC}
15 $\overline{EO}$
14 $\overline{GS}$
13 $\overline{I}_3$
12 $\overline{I}_2$
11 $\overline{I}_1$
10 $\overline{I}_0$
9 $\overline{A}_0$

Logic Symbol



10 11 12 13 1 2 3 4 5
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 EI
EO A_0 A_1 A_2 GS
15 9 7 6 14

V_{CC} = Pin 16
GND = Pin 8

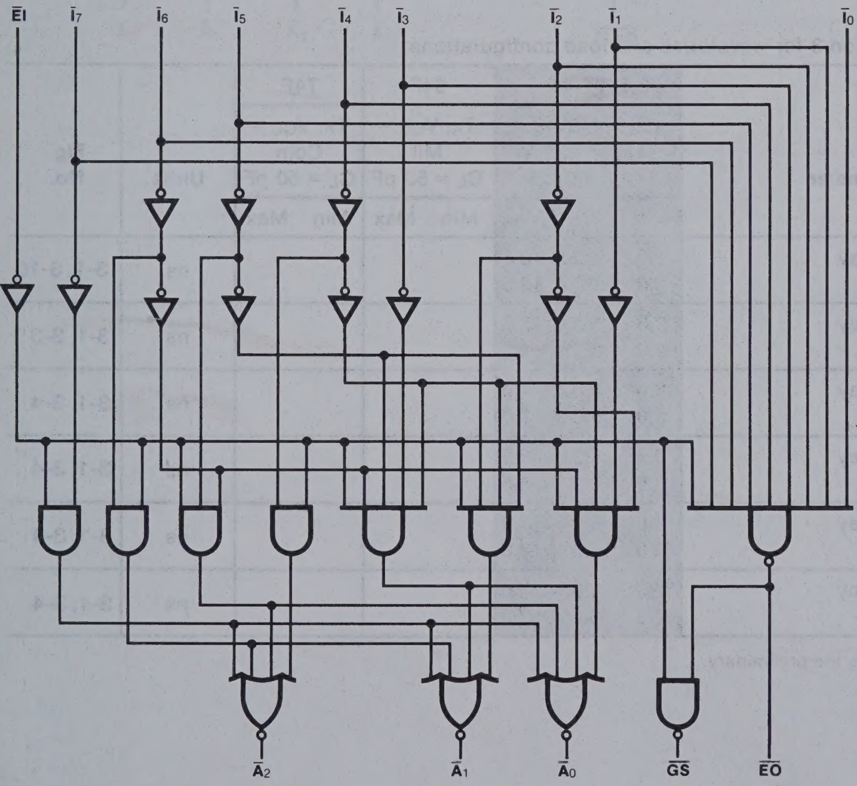
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{I}_0$ - $\overline{I}_7$	Priority Inputs (Active LOW)	0.5/0.375
$\overline{EI}$	Enable Input (Active LOW)	0.5/0.375
$\overline{EO}$	Enable Output (Active LOW)	25/12.5
$\overline{GS}$	Group Select Output (Active LOW)	25/12.5
$\overline{A}_0$ - $\overline{A}_2$	Address Outputs (Active LOW)	25/12.5

Functional Description

The 'F148 8-input priority encoder accepts data from eight active-LOW inputs ($\overline{I_0}$ - $\overline{I_7}$) and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided along with the three priority data outputs ($\overline{A_2}$, $\overline{A_1}$, $\overline{A_0}$). $\overline{GS}$ is active LOW when any input is LOW; this indicates when any input is active. $\overline{EO}$ is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the Enable Input is HIGH.

Logic Diagram



Truth Table

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		23	35	mA	V_{CC} = Max

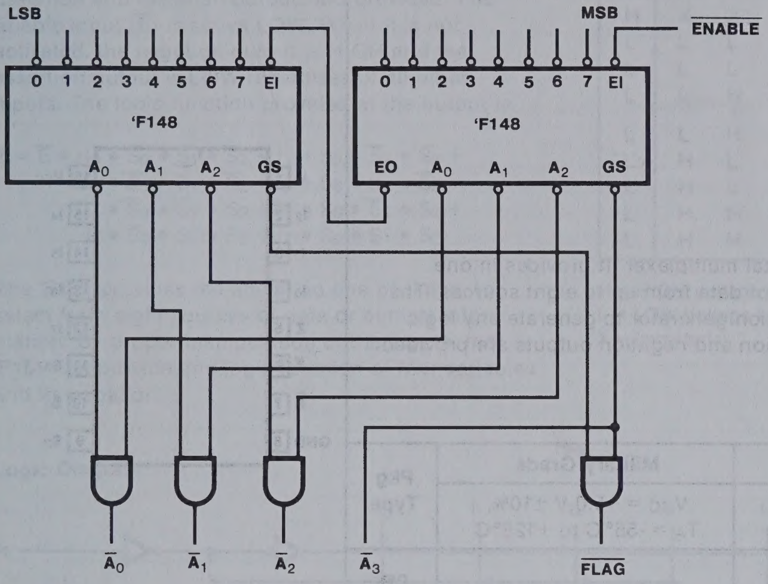
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F ▨			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{A}_n$	3.0 3.0	7.0 7.0	10.5 10.5					ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{EO}$	2.5 2.0	3.5 3.5	5.0 4.5					ns	3-1, 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{GS}$	3.0 3.0	5.0 5.0	7.0 7.0					ns	3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{A}_n$	3.5 3.5	6.0 6.0	8.5 8.5					ns	3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{GS}$	3.0 3.0	5.0 5.0	7.0 7.0					ns	3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$	2.0 2.0	5.0 5.0	7.0 7.0					ns	3-1, 3-4

▨ Test limits in screened columns are preliminary.

Application

16-Input Priority Encoder


LSB
MSB
ENABLE
0
1
2
3
4
5
6
7
EI
'F148
A_0
A_1
A_2
GS
0
1
2
3
4
5
6
7
EI
'F148
EO
A_0
A_1
A_2
GS
$\overline{A}_0$
$\overline{A}_1$
$\overline{A}_2$
$\overline{A}_3$
FLAG

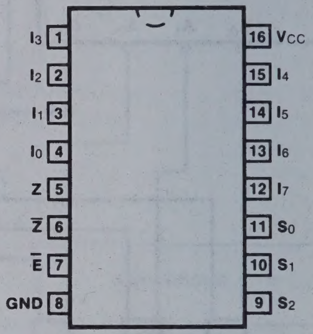
54F/74F151

8-Input Multiplexer

Description

The 'F151 is a high-speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The 'F151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Connection Diagram


I_3 1
I_2 2
I_1 3
I_0 4
Z 5
$\overline{Z}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2

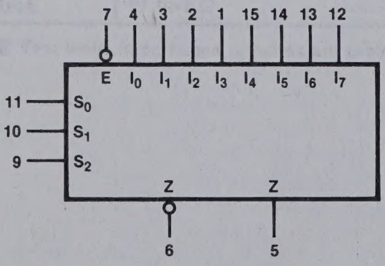
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F151PC		9B
Ceramic DIP (D)	74F151DC	54F151DM	6B
Flatpak (F)		54F151FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$I_0 - I_7$	Data Inputs	0.5/0.375
$S_0 - S_2$	Select Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
Z	Data Output	25/12.5
$\overline{Z}$	Inverted Data Output	25/12.5

Logic Symbol


7
4
3
2
1
15
14
13
12
E
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
11
10
9
S_0
S_1
S_2
Z
Z
6
5

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S_0} \bullet \overline{S_1} \bullet \overline{S_2} + I_1 \bullet S_0 \bullet \overline{S_1} \bullet \overline{S_2} + I_2 \bullet \overline{S_0} \bullet S_1 \bullet \overline{S_2} + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S_2} + I_4 \bullet \overline{S_0} \bullet \overline{S_1} \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S_1} \bullet S_2 + I_6 \bullet \overline{S_0} \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

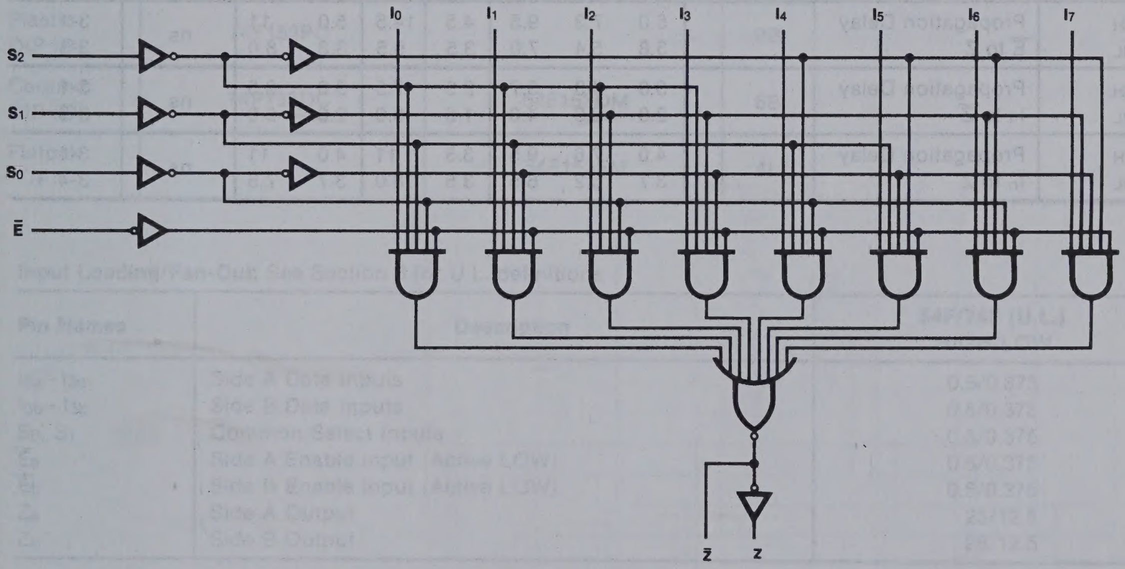
The 'F151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 'F151 can provide any logic function of four variables and its negation.

Truth Table

INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13.5	21	mA	V_{CC} = Max, V_{IN} = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	4.5 3.2	6.2 5.6	8.0 6.1	4.0 3.0	10 8.0	4.5 3.2	9.0 7.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_n to Z	4.5 5.0	9.9 7.1	13 9.0	4.5 4.5	17.5 11.5	4.5 5.0	15 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	3.4 4.5	4.8 6.8	6.1 8.5	3.4 4.0	7.5 10.5	3.4 4.5	7.0 10	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0 3.8	7.3 5.4	9.5 7.0	4.5 3.5	14.5 9.5	5.0 3.8	11 8.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	3.0 2.0	4.3 2.9	5.7 4.0	2.5 1.5	7.5 6.0	3.0 2.0	6.5 5.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	4.0 3.7	7.6 5.2	9.5 6.5	3.5 3.5	11 8.0	4.0 3.7	11 7.5	ns	3-1 3-4

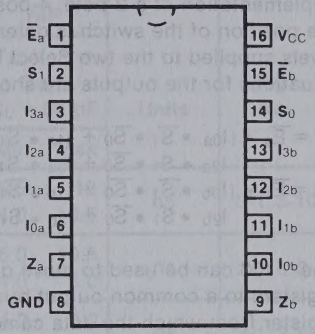
54F/74F153

Dual 4-Input Multiplexer

Description

The 'F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'F153 can generate any two functions of three variables.

Connection Diagram


$\overline{E}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
Z_a 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

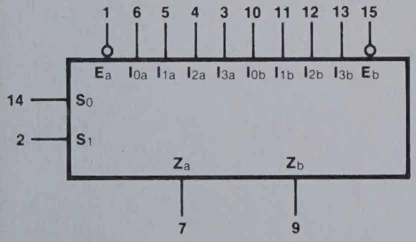
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F153PC		9B
Ceramic DIP (D)	74F153DC	54F153DM	6B
Flatpak (F)		54F153FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
I_{0a} - I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} - I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
Z_a	Side A Output	25/12.5
Z_b	Side B Output	25/12.5

Logic Symbol


1
6
5
4
3
10
11
12
13
15
E_a
I_{0a}
I_{1a}
I_{2a}
I_{3a}
I_{0b}
I_{1b}
I_{2b}
I_{3b}
E_b
14
S_0
2
S_1
Z_a
Z_b
7
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1a} \bullet \overline{S_1} \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S_0} + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1b} \bullet \overline{S_1} \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S_0} + I_{3b} \bullet S_1 \bullet S_0)$$

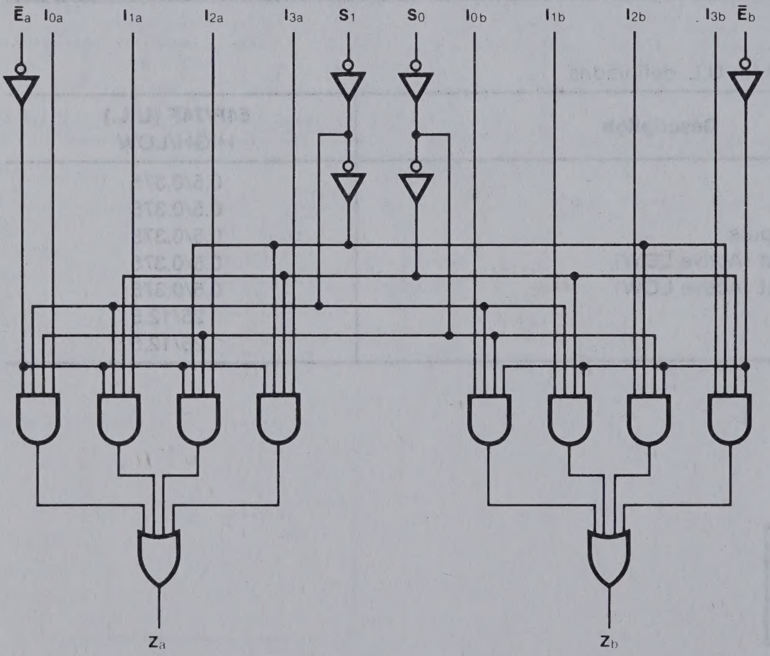
The 'F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

Truth Table

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Description	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	20	mA	V_{CC} = Max, V_{IN} = Gnd

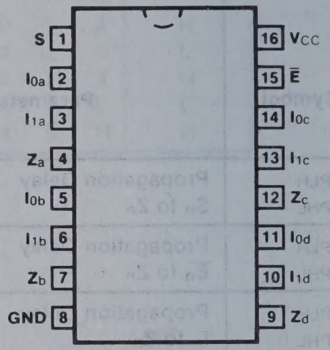
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.5	8.1	10.5	5.0	14	5.5	12	ns	3-1, 3-10
t_{PHL}	S_n to Z_n	4.0	7.0	9.0	3.5	11	4.0	10.5		
t_{PLH}	Propagation Delay	5.0	7.1	9.0	4.5	11.5	5.0	10.5	ns	3-1, 3-3
t_{PHL}	$\overline{E}_n$ to Z_n	4.0	5.7	7.0	3.5	9.0	4.0	8.0		
t_{PLH}	Propagation Delay	4.0	5.3	7.0	3.5	9.0	4.0	8.0	ns	3-1, 3-4
t_{PHL}	I_n to Z_n	3.0	5.1	6.5	2.5	8.0	3.0	7.5		

54F/74F157

Quad 2-Input Multiplexer

Connection Diagram


S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

Description

The 'F157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157 can also be used to generate any four of the 16 different functions to two variables.

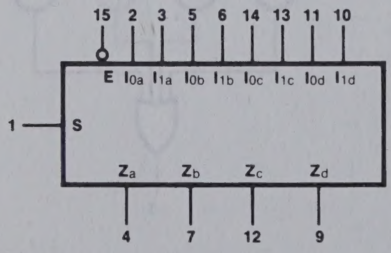
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F157PC		9B
Ceramic DIP (D)	74F157DC	54F157DM	6B
Flatpak (F)		54F157FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$I_{0a}-I_{0d}$	Source 0 Data Inputs	0.5/0.375
$I_{1a}-I_{1d}$	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
Z_a-Z_d	Outputs	25/12.5

Logic Symbol


15
2
3
5
6
14
13
11
10
E
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
1
S
Z_a
Z_b
Z_c
Z_d
4
7
12
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'F157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$ $Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

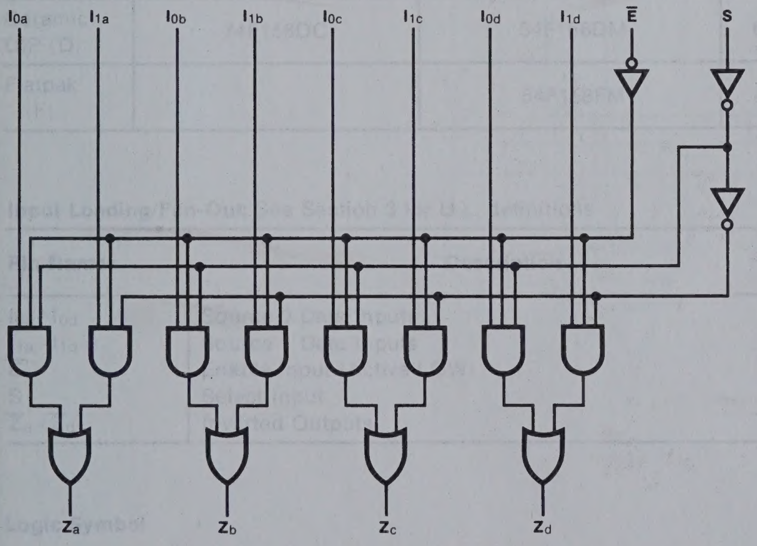
A common use of the 'F157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

Truth Table

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = Max, All Inputs = 4.5 V

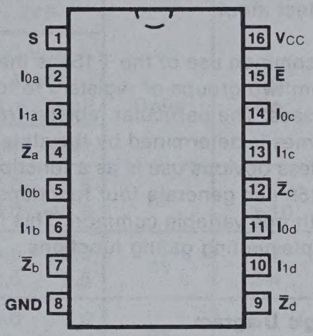
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	4.5	10.1	13	3.5	17	4.5	15	ns	3-1
t_{PHL}		3.5	6.3	8.0	3.5	11.5	3.5	9.0		3-10
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	5.0	7.6	10	5.0	15	5.0	11.5	ns	3-1
t_{PHL}		3.8	5.3	7.0	3.8	8.5	3.8	8.0		3-3
t_{PLH}	Propagation Delay I_n to Z_n	3.8	5.5	7.0	3.5	10	3.8	8.0	ns	3-1
t_{PHL}		2.5	4.6	5.5	2.5	7.5	2.5	7.0		3-4

54F/74F158

Quad 2-Input Multiplexer

Connection Diagram


S 1
I_{0a} 2
I_{1a} 3
$\overline{Z}_a$ 4
I_{0b} 5
I_{1b} 6
$\overline{Z}_b$ 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 $\overline{Z}_c$
11 I_{0d}
10 I_{1d}
9 $\overline{Z}_d$

Description

The 'F158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'F158 can also generate any four of the 16 different functions of two variables.

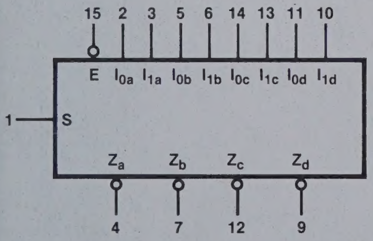
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F158PC		9B
Ceramic DIP (D)	74F158DC	54F158DM	6B
Flatpak (F)		54F158FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$I_{0a} - I_{0d}$	Source 0 Data Inputs	0.5/0.375
$I_{1a} - I_{1d}$	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs	25/12.5

Logic Symbol


15
2
3
5
6
14
13
11
10
E
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
1
S
Z_a
Z_b
Z_c
Z_d
4
7
12
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'F158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

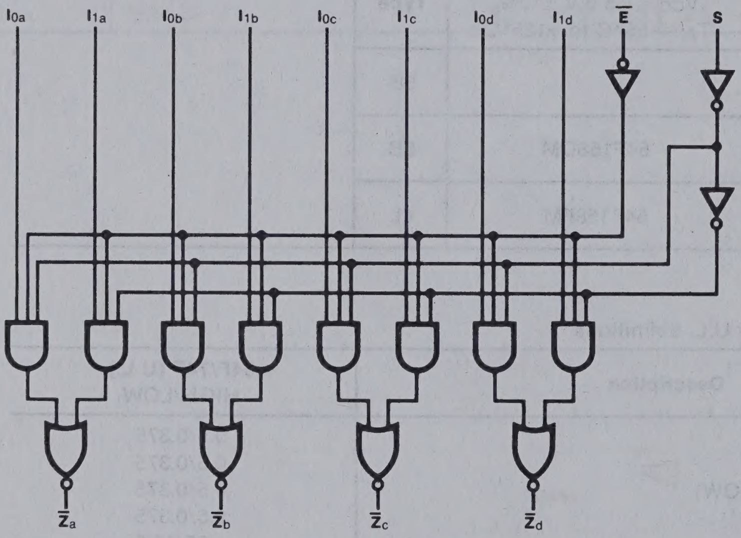
A common use of the 'F158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

INPUTS				OUTPUTS
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		10	15	mA	V_{CC} = Max*

AC Characteristics: See Section 3 for waveforms and load configurations

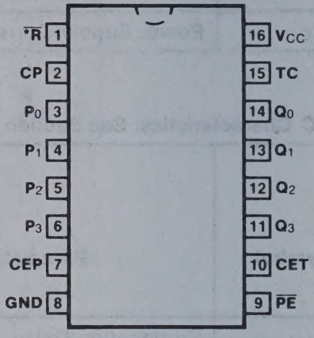
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	4.0	6.4	8.5	4.0	10.5	4.0	9.5	ns	3-1
t_{PHL}	S to $\overline{Z}$	4.0	6.9	9.0	4.0	10.5	4.0	10.5		3-10
t_{PLH}	Propagation Delay	4.5	6.2	8.0	4.5	9.5	4.5	9.0	ns	3-1
t_{PHL}	$\overline{E}$ to $\overline{Z}$	3.5	6.4	8.5	3.5	9.5	3.5	9.5		3-4
t_{PLH}	Propagation Delay	3.0	4.4	5.9	2.5	8.5	3.0	7.0	ns	3-1
t_{PHL}	I_n to $\overline{Z}$	2.0	3.3	4.5	2.0	6.0	2.0	5.5		3-3

*I_{CC} measured with outputs open and 4.5 V applied to all inputs.

54F/74F160 • 54F/74F162

Synchronous Presettable BCD Decade Counter

Connection Diagram



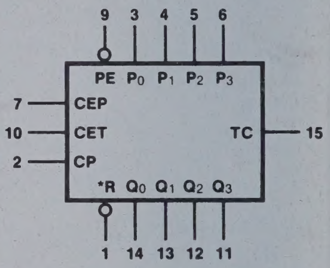
*$\overline{\text{MR}}$ for '160
*$\overline{\text{SR}}$ for '162

Description

The 'F160 and 'F162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- **Synchronous Counting and Loading**
- **High-speed Synchronous Expansion**
- **Typical Count Rate of 125 MHz**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

*$\overline{\text{MR}}$ for '160
*$\overline{\text{SR}}$ for '162

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = −55° C to +125° C	
Plastic DIP (P)	74F160PC, 74F162PC		9B
Ceramic DIP (D)	74F160DC, 74F162DC	54F160DM, 54F162DM	7B
Flatpak (F)		54F160FM, 54F162FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{\text{MR}}$ ('F160)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{\text{SR}}$ ('F162)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0 - P_3	Parallel Data Inputs	0.5/0.375
$\overline{\text{PE}}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0 - Q_3	Flip-flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

Functional Description

The 'F160 and 'F162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160), synchronous reset ('F162), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{\text{MR}}$, 'F160), Synchronous Reset ($\overline{\text{SR}}$, 'F162), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{\text{PE}}$ and $\overline{\text{MR}}$ ('F160) or $\overline{\text{SR}}$ ('F162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F160 and 'F162 use D-type edge-triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160, 'F162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

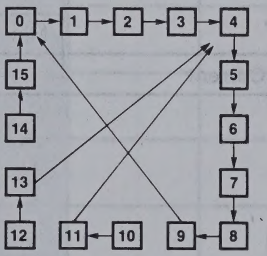
Logic Equations: Count Enable = CEP • CET • PE
TC = $Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$ • CET

Mode Select Table

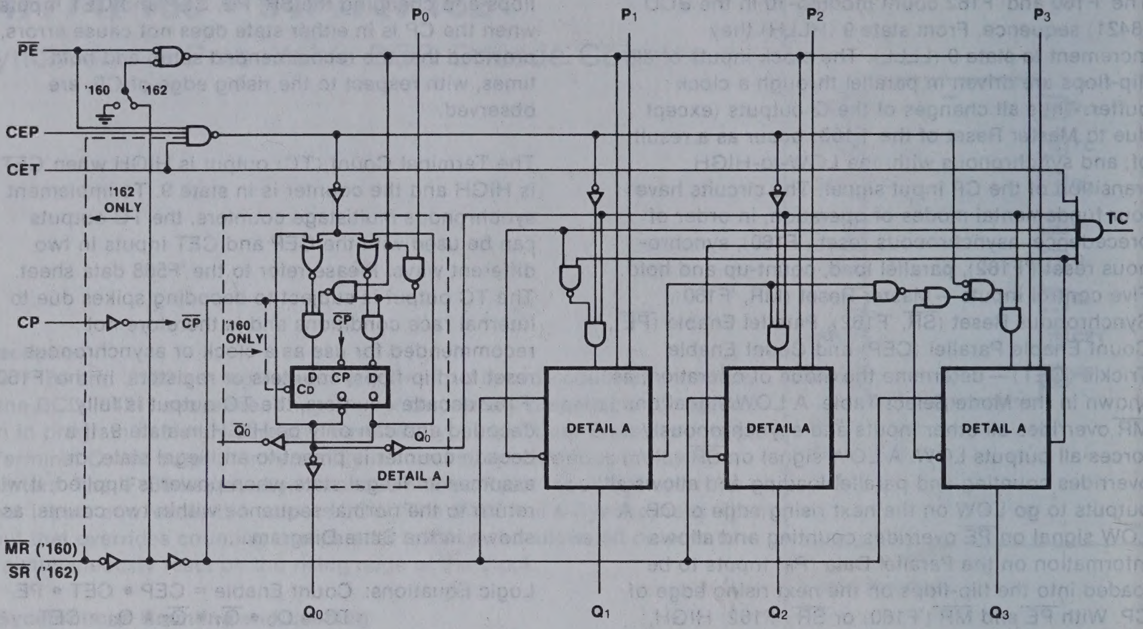
*$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 'F162 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram


P0
P1
P2
P3
PE
'160
'162
CEP
CET
'162 ONLY
CP
CP
'160 ONLY
D CP D
CD
Q Q
Q'0
Q0
DETAIL A
DETAIL A
DETAIL A
DETAIL A
TC
MR ('160)
SR ('162)
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	50	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125						MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.0 4.0	5.0 7.0	7.0 10					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	4.0 5.0	7.0 8.0	10 11						
t_{PLH} t_{PHL}	Propagation Delay CP to TC	6.0 5.5	10 9.0	14 12.5					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 3.0	4.0 5.0	5.5 7.0					ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F160)	6.0	10	14					ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

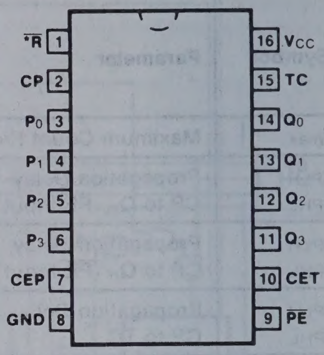
Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	3.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	3.0 3.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	10 7.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP or CET to CP	10 4.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP or CET to CP	0 0								
t_w (H) t_w (L)	Clock Pulse Width, HIGH or LOW	4.0 5.0							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW ('F160)	6.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F160)	5.0								

▨ Test limits in screened columns are preliminary.

54F/74F161 • 54F/74F163

Synchronous Presettable Binary Counter

Connection Diagram



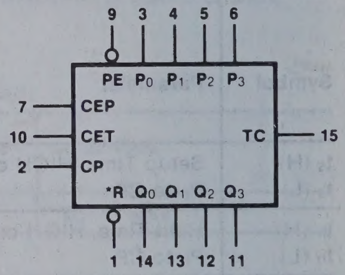
*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

Description

The 'F161 and 'F163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- **Synchronous Counting and Loading**
- **High Speed Synchronous Expansion**
- **Typical Count Frequency of 125 MHz**

Logic Symbol



*$\overline{MR}$ for '161 V_{CC} = Pin 16
*$\overline{SR}$ for '163 GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0 \pm 5\%$, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0$ V $\pm 10\%$, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F161PC, 74F163PC		9B
Ceramic DIP (D)	74F161DC, 74F163DC	54F161DM, 54F163DM	7B
Flatpak (F)		54F161FM, 54F163FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F161)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F163)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0-Q_3	Flip-flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

Functional Description

The 'F161 and 'F163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F161), synchronous reset ('F163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{\text{MR}}$, 'F161), Synchronous Reset ($\overline{\text{SR}}$, 'F163), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip- flops on the next rising edge of CP. With $\overline{\text{PE}}$ and $\overline{\text{MR}}$ ('F161) or $\overline{\text{SR}}$ ('F163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

Mode Select Table

*$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

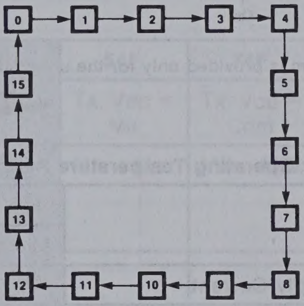
*For 'F163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

The 'F161 and 'F163 use D-type edge-triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

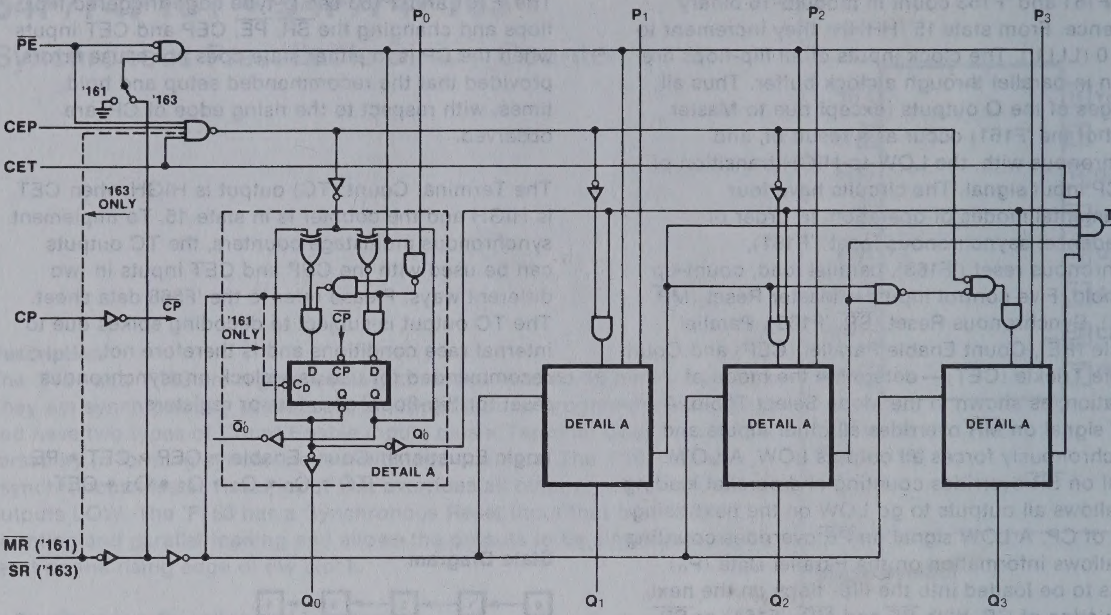
The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • PE
TC = Q_0 • Q_1 • Q_2 • Q_3 • CET

State Diagram



Logic Diagram



$\overline{PE}$
'161
'163
CEP
CET
'163 ONLY
CP
$\overline{CP}$
'161 ONLY
D
CP
D
C_D
Q
Q
$\overline{CP}$
$\overline{Q}_0$
Q_0
DETAIL A
$\overline{MR}$ ('161)
$\overline{SR}$ ('163)
P_0
P_1
P_2
P_3
TC
DETAIL A
DETAIL A
DETAIL A
Q_0
Q_1
Q_2
Q_3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	50	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125						MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.0 4.0	5.0 7.0	7.0 10					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	4.0 5.0	7.0 8.0	10 11						
t_{PLH} t_{PHL}	Propagation Delay CP to TC	6.0 5.5	10 9.0	14 12.5					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 3.0	4.0 5.0	5.5 7.0					ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161)	6.0	10	14					ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

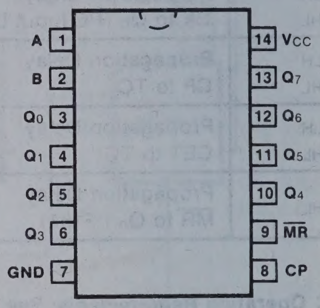
Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	3.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	3.0 3.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	10 7.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP or CET to CP	10 4.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP or CET to CP	0 0								
t_w (H) t_w (L)	Clock Pulse Width, HIGH or LOW	4.0 5.0							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW ('F161)	6.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F161)	5.0								

▨ Test limits in screened columns are preliminary.

54F/74F164

Serial-In Parallel-Out Shift Register

Connection Diagram



Description

The 'F164 is a high speed 8-bit serial-in parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

- **Typical shift Frequency of 90 MHz**
- **Asynchronous Master Reset**
- **Gated Serial Data Input**
- **Fully Synchronous Data Transfers**

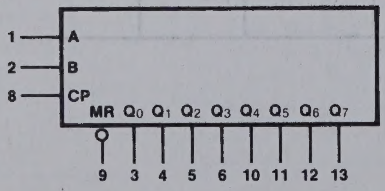
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F164PC		9A
Ceramic DIP (D)	74F164DC	54F164DM	6A
Flatpak (F)		54F164FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
A, B	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$Q_0 - Q_7$	Outputs	25/12.5

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

Functional Description

The 'F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active-HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

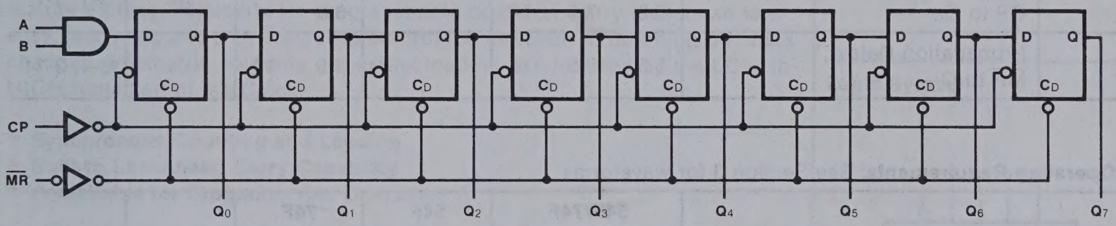
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L — L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	55	mA	A, B = GND, V_{CC} = Max, CP = 2.4 V, $\overline{MR}$ = _┌

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	90				80		MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	4.5 5.0	6.0 7.5	8.0 10			4.5 5.0	9.0 11	ns	3-1, 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.5	10.5	13			8.5	14	ns	3-1, 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A or B to CP	7.0 7.0					7.0 7.0		ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW A or B to CP	1.0 1.0					1.0 1.0			
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 7.0					4.0 7.0		ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	7.0					7.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0					7.0		ns	3-11

54F/74F168 • 54F/74F169

4-Stage Synchronous Bidirectional Counters

Description

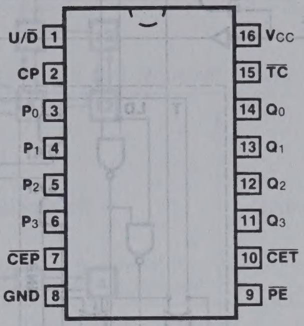
The ’F168 and ’F169 are fully synchronous 4-stage up/down counters. The ’F168 is a BCD decade counter; the ’F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operaton, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

- **Synchronous Counting and Loading**
- **Built-in Lookahead Carry Capability**
- **Presettable for Programmable Operation**

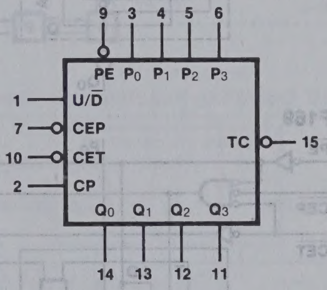
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 ±5%, T_A = 0° C to +70° C	V_{CC} = + 5.0 V ±10%, T_A = −55° C to +125° C	
Plastic DIP (P)	74F168PC, 74F169PC		9B
Ceramic DIP (D)	74F168DC, 74F169DC	54F168DM, 54F169DM	6B
Flatpak (F)		54F168FM, 54F169FM	4L

Connection Diagram


U/$\overline{D}$ 1
CP 2
P0 3
P1 4
P2 5
P3 6
$\overline{CEP}$ 7
GND 8
16 VCC
15 $\overline{TC}$
14 Q0
13 Q1
12 Q2
11 Q3
10 $\overline{CET}$
9 $\overline{PE}$

Logic Symbol


9 3 4 5 6
PE P0 P1 P2 P3
1 U/D
7 CEP
10 CET
2 CP
TC 15
Q0 Q1 Q2 Q3
14 13 12 11

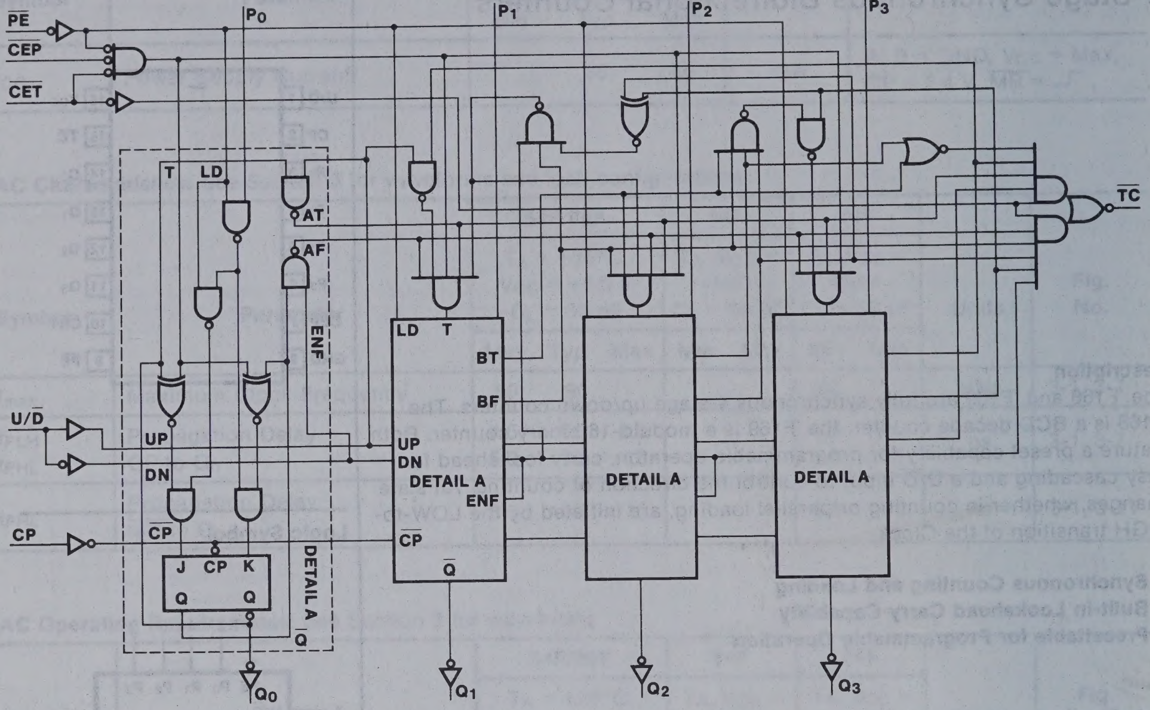
V_{CC} = Pin 16
GND = Pin 8

Input Loading/Fan-Out: See Section 3 for U.L. definitions

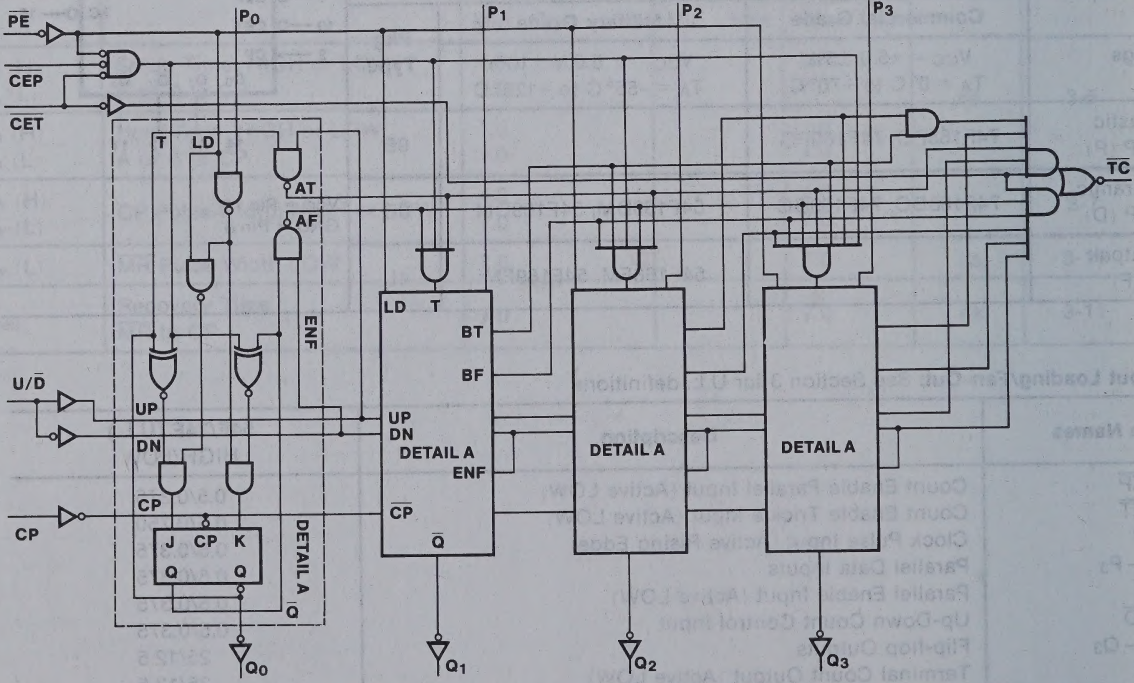
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.750
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Logic Diagrams

'F168


PE
CEP
CET
P0
P1
P2
P3
T
LD
AT
AF
ENF
U/D
UP
DN
CP
CP
J
CP
K
Q
Q
DETAIL A
Q
LD
T
BT
BF
UP
DN
DETAIL A
ENF
CP
Q
DETAIL A
DETAIL A
TC
Q0
Q1
Q2
Q3

'F169


PE
CEP
CET
P0
P1
P2
P3
T
LD
AT
AF
ENF
U/D
UP
DN
CP
CP
J
CP
K
Q
Q
DETAIL A
Q
LD
T
BT
BF
UP
DN
DETAIL A
ENF
CP
Q
DETAIL A
DETAIL A
TC
Q0
Q1
Q2
Q3

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F168 and 'F169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{\text{PE}}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ must be LOW and $\overline{\text{PE}}$ must be HIGH; the $U/\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{\text{TC}}$) output is normally HIGH and goes LOW, provided that $\overline{\text{CET}}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the Count Up mode. The $\overline{\text{TC}}$ output state is not a function of the Count Enable Parallel ($\overline{\text{CEP}}$) input level. The $\overline{\text{TC}}$ output of the 'F168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{\text{TC}}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{\text{TC}}$. For this reason the use of $\overline{\text{TC}}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{\text{CEP}} \bullet \overline{\text{CET}} \bullet \overline{\text{PE}}$
2) Up: $\overline{\text{TC}} = Q_0 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{\text{CET}}$
3) Down: $\overline{\text{TC}} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{\text{CET}}$

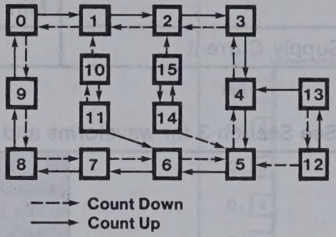
Mode Select Table

$\overline{\text{PE}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

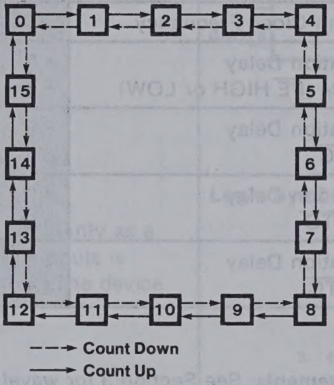
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

'F168



'F169



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	52	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	75							MHz	3-1, 3-7
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	4.0	7.0	10					ns	3-1, 3-7
t_{PHL}		5.5	9.0	12.5						
t_{PLH}	Propagation Delay CP to $\overline{TC}$	6.5	10.5	15					ns	3-1, 3-7
t_{PHL}		6.5	10.5	15						
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	4.0	6.5	9.0					ns	3-1, 3-4
t_{PHL}		3.5	5.5	8.0						
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	4.0	6.5	9.0					ns	3-1, 3-10
t_{PHL}		4.5	7.5	10						

AC Operating Requirements: See Section 3 for waveforms

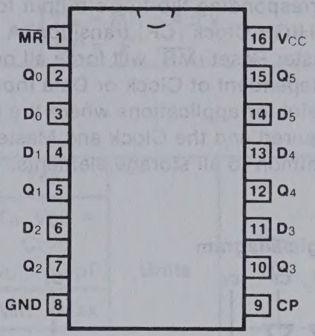
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW P_n to CP	5.0							ns	3-5
t_s (L)		7.0								
t_h (H)	Hold Time, HIGH or LOW P_n to CP	3.0								
t_h (L)		3.0								
t_s (H)	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	10							ns	3-5
t_s (L)		10								
t_h (H)	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0								
t_h (L)		0								
t_s (H)	Setup Time, HIGH or LOW U/$\overline{D}$ or $\overline{PE}$ to CP	14							ns	3-5
t_s (L)		14								
t_h (H)	Hold Time, HIGH or LOW U/$\overline{D}$ or $\overline{PE}$ to CP	0								
t_h (L)		0								
t_w (H)	CP Pulse Width, HIGH or LOW	4.5							ns	3-7
t_w (L)		6.5								

▨ Test limits in screened columns are preliminary.

54F/74F174

Hex D Flip-Flop
(With Master Reset)

Connection Diagram

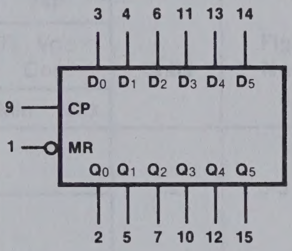

$\overline{MR}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
D_2 6
Q_2 7
GND 8
9 CP
10 Q_3
11 D_3
12 Q_4
13 D_4
14 D_5
15 Q_5
16 V_{CC}

Description

The 'F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Asynchronous Common Reset**

Logic Symbol


3
4
6
11
13
14
D_0
D_1
D_2
D_3
D_4
D_5
9
CP
1
MR
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
2
5
7
10
12
15

V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F174PC		9B
Ceramic DIP (D)	74F174DC	54F174DM	6B
Flatpak (F)		54F174FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$D_0 - D_5$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$Q_0 - Q_5$	Outputs	25/12.5

Functional Description

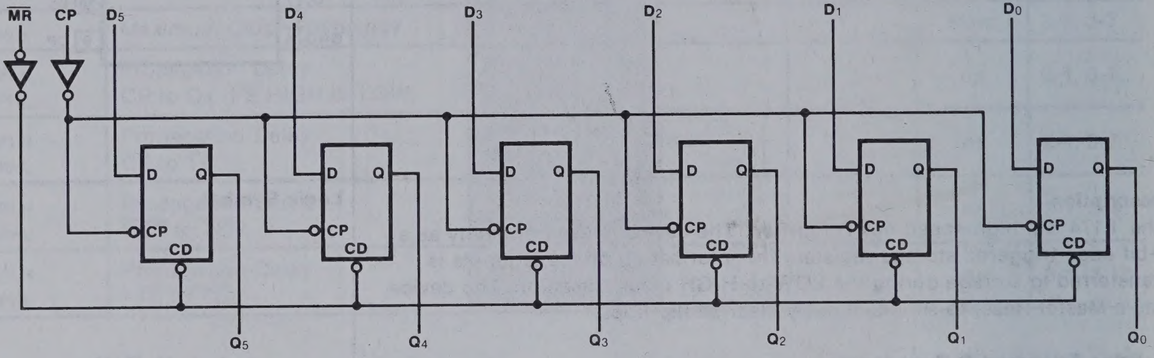
The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ t_{n+1}
D_n	Q_n
H L	H L

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max, $D_n = \overline{MR}$ = 4.5 V CP = ⎍

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140						MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 4.5	5.5 7.0	8.0 10					ns	3-1, 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	10	14					ns	3-1, 3-11

AC Operating Requirements: See Section 3 for waveforms

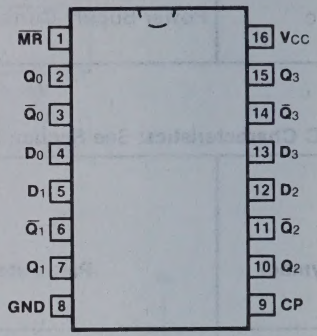
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	4.0 4.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	1.0 1.0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 5.0							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0							ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F175

Quad D Flip-Flop

Connection Diagram

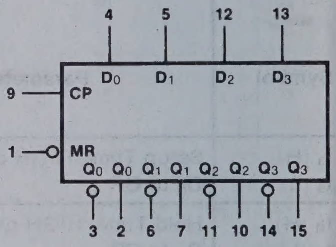

$\overline{MR}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP

Description

The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **Asynchronous Common Reset**
- **True and Complement Output**

Logic Symbol


4
5
12
13
D_0
D_1
D_2
D_3
9
CP
1
MR
Q_0
$\overline{Q}_0$
Q_1
$\overline{Q}_1$
Q_2
$\overline{Q}_2$
Q_3
$\overline{Q}_3$
3
2
6
7
11
10
14
15

V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0$ V $\pm 5\%$, $T_A = 0°$C to $+70°$C	$V_{CC} = +5.0$ V $\pm 10\%$, $T_A = -55°$C to $+125°$C	
Plastic DIP (P)	74F175PC		9B
Ceramic DIP (D)	74F175DC	54F175DM	6B
Flatpak (F)		54F175FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$D_0 - D_3$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$Q_0 - Q_3$	True Outputs	25/12.5
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	25/12.5

Functional Description

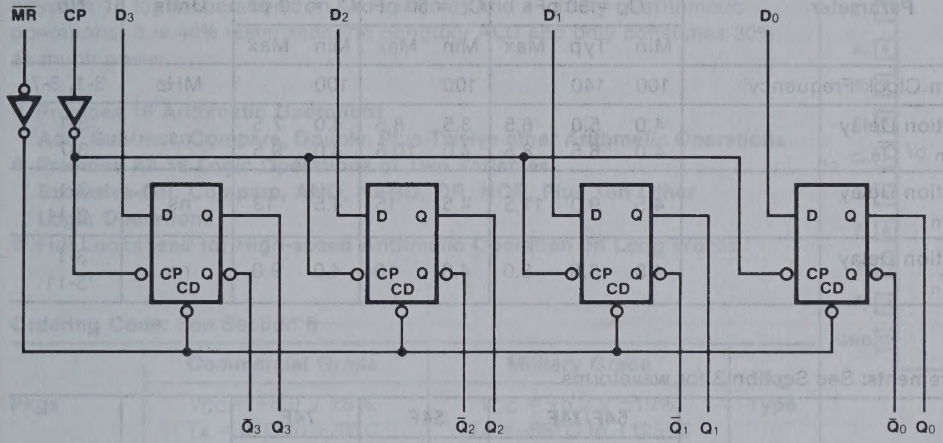
The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

INPUTS	OUTPUTS	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

t_n = Bit time before clock positive-going transition
t_{n+1} = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		22.5	34	mA	V_{CC} = Max $D_n = \overline{MR}$ = 4.5 V CP = _⌐

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140		100		100		MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	4.0 4.0	7.5 9.5	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	9.0	11.5	4.5	15	4.5	13	ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.0	4.0	10	4.0	9.0	ns	3-1 3-11

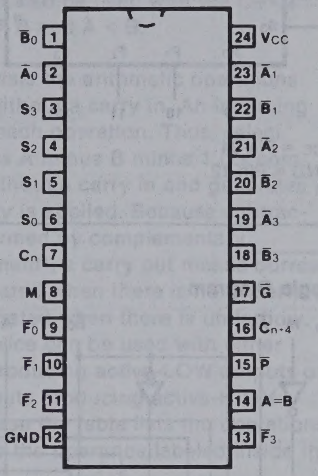
AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	1.0 1.0			1.0 1.0		1.0 1.0			
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0			5.0		5.0		ns	3-11

54F/74F181

4-Bit Arithmetic Logic Unit

Connection Diagram



$\overline{B}_0$ 1
$\overline{A}_0$ 2
S_3 3
S_2 4
S_1 5
S_0 6
C_n 7
M 8
$\overline{F}_0$ 9
$\overline{F}_1$ 10
$\overline{F}_2$ 11
GND 12
24 V_{CC}
23 $\overline{A}_1$
22 $\overline{B}_1$
21 $\overline{A}_2$
20 $\overline{B}_2$
19 $\overline{A}_3$
18 $\overline{B}_3$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A=B
13 $\overline{F}_3$

4

Description

The 'F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

- **Provides 16 Arithmetic Operations**
  Add, Subtract, Compare, Double, Plus Twelve other Arithmetic Operations
- **Provides All 16 Logic Operations of Two Variables**
  Exclusive-OR, Compare, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- **Full Lookahead for High-speed Arithmetic Operation on Long Words**

Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F181PC		9N
Ceramic DIP (D)	74F181DC	54F181DM	6N
Flatpak (F)		54F181FM	4M

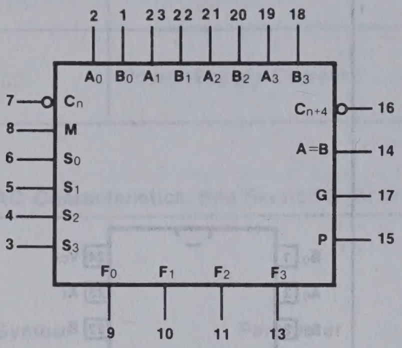
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{A}_0$ - $\overline{A}_3$	A Operand Inputs (Active LOW)	0.5/1.125
$\overline{B}_0$ - $\overline{B}_3$	B Operand Inputs (Active LOW)	0.5/1.125
S_0 - S_3	Function Select Inputs	0.5/1.50
M	Mode Control Input	0.5/0.375
C_n	Carry Input	0.5/1.875
$\overline{F}_0$ - $\overline{F}_3$	Function Outputs (Active LOW)	25/12.5
A = B	Comparator Output	OC*/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5
C_{n+4}	Carry Output	25/12.5

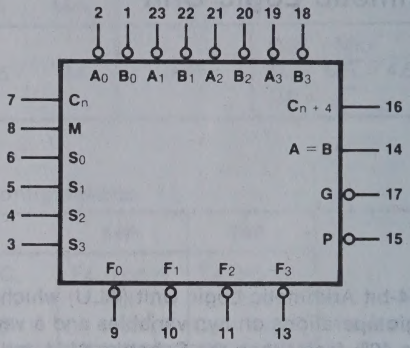
*OC—Open Collector

Logic Symbols

Active-HIGH Operands

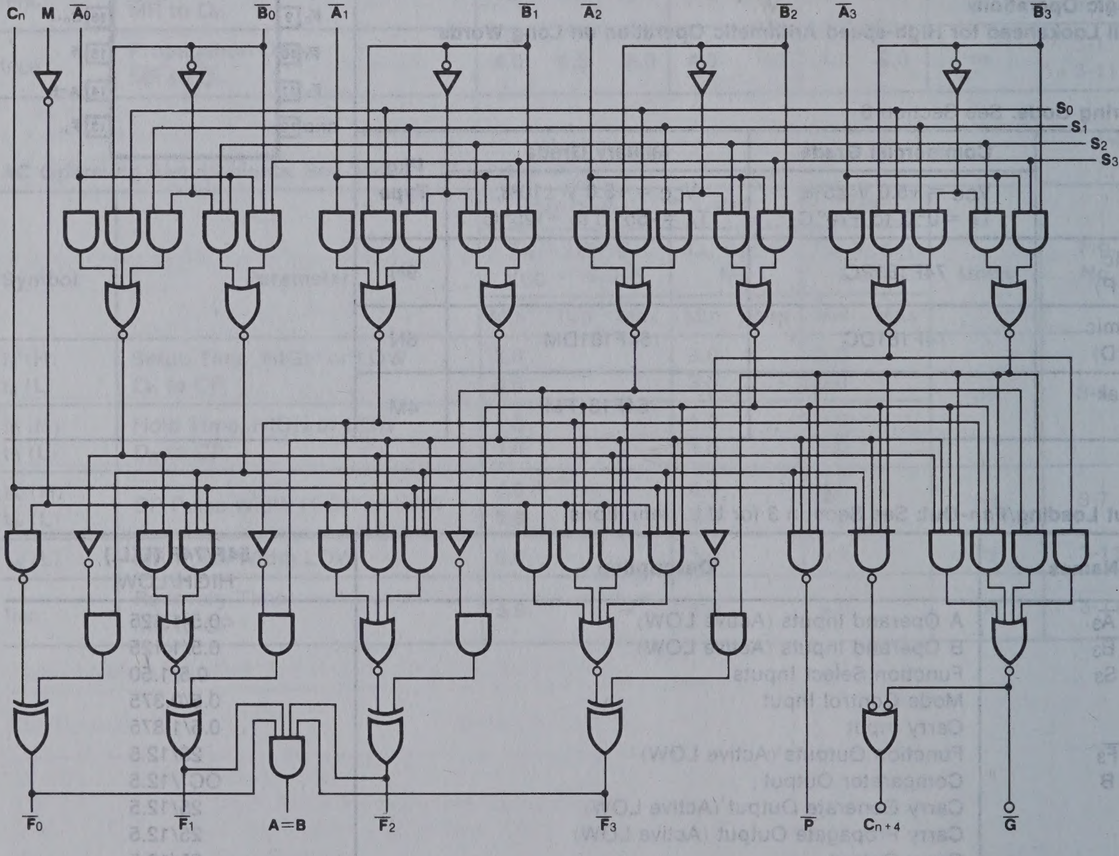

2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7
Cn
8
M
6
S0
5
S1
4
S2
3
S3
Cn+4
16
A=B
14
G
17
P
15
F0
F1
F2
F3
9
10
11
13

Active-LOW Operands


2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7
Cn
8
M
6
S0
5
S1
4
S2
3
S3
Cn + 4
16
A = B
14
G
17
P
15
F0
F1
F2
F3
9
10
11
13

V_{CC} = Pin 24
GND = Pin 12

Logic Diagram


Cn
M
$\overline{A}_0$
$\overline{B}_0$
$\overline{A}_1$
$\overline{B}_1$
$\overline{A}_2$
$\overline{B}_2$
$\overline{A}_3$
$\overline{B}_3$
S0
S1
S2
S3
$\overline{F}_0$
$\overline{F}_1$
A=B
$\overline{F}_2$
$\overline{F}_3$
$\overline{P}$
Cn+4
$\overline{G}$

Functional Description

The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

MODE SELECT INPUTS				ACTIVE-LOW OPERANDS & F_n OUTPUTS		ACTIVE-HIGH OPERANDS & F_n OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A}+B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position
**arithmetic operations expressed in 2s complement notation

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{OH}	Output HIGH Current			250	μA	V_{OH} = 4.5 V, V_{CC} = Min, A = B
I_{CC}	Power Supply Current		43	65	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter		54F/74F			54F		74F		Units	Fig. No.
			T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	C_n to C_{n+4}		3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	12 11.5	3.0 3.0	9.5 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	7.0 7.0	10 9.4	13 12	7.0 7.0	18 17	7.0 7.0	14 13	ns	3-1 3-3
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	7.0 7.0	10.8 10	14 13	7.0 7.0	19.5 18	7.0 7.0	15 14	ns	3-1 3-3
t_{PLH} t_{PHL}	C_n to $\overline{F}$	Any	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	12 12	3.0 3.0	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Sum	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	10.5 10.5	3.0 3.0	8.5 8.5	ns	3-4 3-4
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	12 13.5	3.0 3.0	9.5 10.5	ns	3-1 3-3
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	10 10.5	3.0 3.0	8.0 8.5	ns	3-1 3-3
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	10.5 12	4.0 4.0	8.5 9.5	ns	3-1 3-3
t_{PLH} t_{PHL}	$\overline{A_i}$ to $\overline{B_i}$ to $\overline{F_i}$	Sum	4.0 4.0	7.0 7.2	9.0 10	4.0 4.0	12.5 14	4.0 4.0	10 10	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	$\overline{A_i}$ or $\overline{B_i}$ to $\overline{F_i}$	Dif	4.5 4.5	8.2 5.0	11 11	4.5 4.5	15.5 15.5	4.5 4.5	12 12	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0 4.0	8.0 7.8	10.5 10	4.0 4.0	15.5 14	4.0 4.0	11.5 11	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	4.5 4.5	9.4 9.4	12 12	4.5 4.5	17 17	4.5 4.5	13 13	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0 4.0	6.0 6.0	9.0 10	4.0 4.0	12.5 14	4.0 4.0	10 11	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to A = B	Dif	11 7.0	18.5 9.8	27 12.5	11 7.0	35 17.5	11 7.0	29 13.5	ns	3-1, 3-3 3-4

▨ Test limits in screened columns are preliminary.

54F/74F182

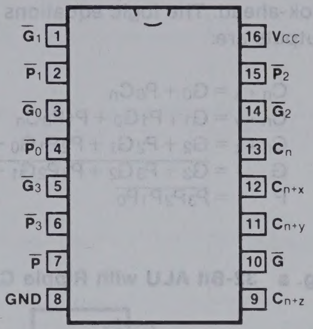
Carry Lookahead Generator

Description

The 'F182 is a high-speed carry lookahead generator. It is generally used with the 'F181, 'F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

- **Provides Lookahead Carries across a Group of Four ALUs**
- **Multi-level Lookahead High-speed Arithmetic Operation over Long Word Lengths**

Connection Diagram



$\overline{G}_1$ 1
$\overline{P}_1$ 2
$\overline{G}_0$ 3
$\overline{P}_0$ 4
$\overline{G}_3$ 5
$\overline{P}_3$ 6
$\overline{P}$ 7
GND 8
16 V_{CC}
15 $\overline{P}_2$
14 $\overline{G}_2$
13 C_n
12 C_{n+x}
11 C_{n+y}
10 $\overline{G}$
9 C_{n+z}

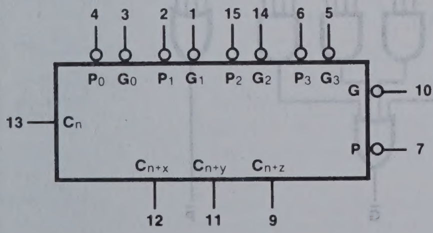
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F182PC		9B
Ceramic DIP (D)	74F182DC	54F182DM	7B
Flatpak (F)		54F182FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
C_n	Carry Input	0.5/0.75
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	0.5/5.25
$\overline{G}_1$	Carry Generate Input (Active LOW)	0.5/6.0
$\overline{G}_3$	Carry Generate Input (Active LOW)	0.5/3.0
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	0.5/3.0
$\overline{P}_2$	Carry Propagate Input (Active LOW)	0.5/2.25
$\overline{P}_3$	Carry Propagate Input (Active LOW)	0.5/1.5
$C_{n+x} - C_{n+z}$	Carry Outputs	25/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5

Logic Symbol



4
3
2
1
15
14
6
5
P_0
G_0
P_1
G_1
P_2
G_2
P_3
G_3
G
10
P
7
13
C_n
C_{n+x}
C_{n+y}
C_{n+z}
12
11
9

V_{CC} = Pin 16
GND = Pin 8

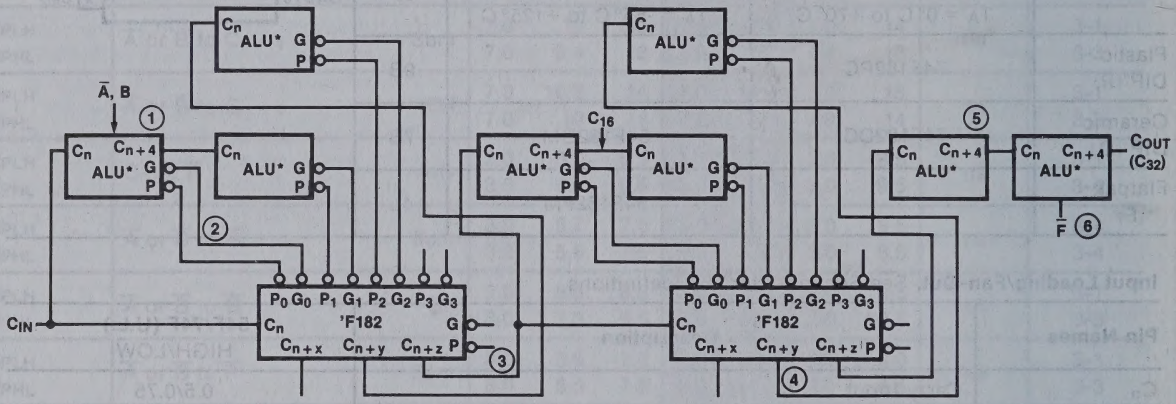
Functional Description

The 'F182 carry lookahead generator accepts up to four pairs of active-LOW Carry Propagate ($\overline{P}_0 - \overline{P}_3$) and Carry Generate ($\overline{G}_0 - \overline{G}_3$) signals and an active-HIGH Carry input (C_n) and provides anticipated active-HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active-LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of look-ahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G \quad = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$P \quad = \overline{P_3P_2P_1P_0}$$

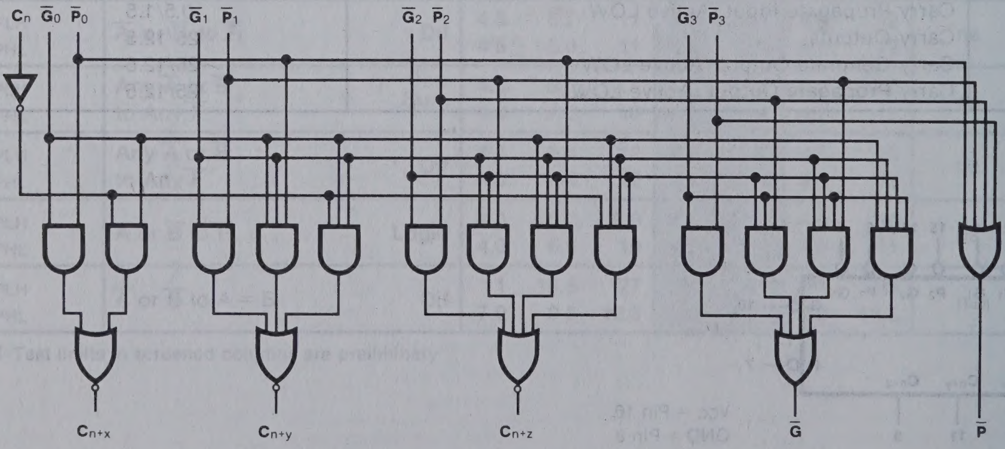
Also, the 'F182 can be used with binary ALU's in an active-LOW or active-HIGH input operand mode. The connections *(Figure a)* to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 'F181 or 'F381.

Fig. a 32-Bit ALU with Ripple Carry between 16-Bit Lookahead ALUs



*ALUs may be either 'F181, 'F381 or 2901A

Logic Diagram



Truth Table

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current (All Outputs HIGH)		18.4	28	mA	V_{CC} = Max; $\overline{P}_3$, $\overline{G}_3$ = 4.5 V All Other Inputs = Gnd
I_{CCL}	Power Supply Current (All Outputs LOW)		23.5	36	mA	V_{CC} = Max; $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V All Other Inputs = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

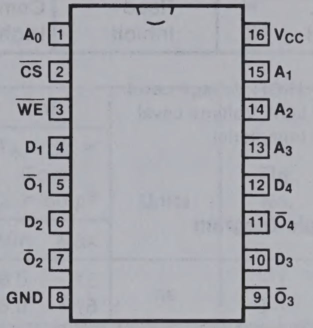
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	10.5	3.0	9.5	ns	3-1
t_{PHL}	C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0	6.8	9.0	3.0	11	3.0	10		3-4
t_{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	10.7	2.5	9.0	ns	3-1
t_{PHL}	$\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	2.0	3.7	5.0	2.0	6.5	2.0	6.0		3-3
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	10.5	2.5	9.5	ns	3-1
t_{PHL}	$\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	2.0	3.9	5.2	2.0	6.5	2.0	6.0		3-3
t_{PLH}	Propagation Delay	3.0	7.9	10.0	3.0	12.5	3.0	11	ns	3-1
t_{PHL}	$\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	3.0	6.0	8.0	3.0	9.5	3.0	9.0		3-4
t_{PLH}	Propagation Delay	3.0	8.3	10.5	3.0	12.5	3.0	11.5	ns	3-1
t_{PHL}	$\overline{G}_n$ to $\overline{G}$	3.0	5.7	7.5	3.0	9.5	3.0	8.5		3-4
t_{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	11	3.0	8.5	ns	3-1
t_{PHL}	$\overline{P}_n$ to $\overline{P}$	2.5	4.1	5.5	2.5	7.5	2.5	6.5		3-4

▨ Test limits in screened columns are preliminary.

54F/74F189

64-Bit Random Access Memory
(With 3-State Outputs)

Connection Diagram

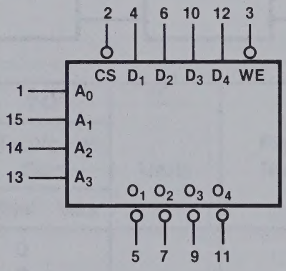

A0 1
CS 2
WE 3
D1 4
O1 5
D2 6
O2 7
GND 8
16 VCC
15 A1
14 A2
13 A3
12 D4
11 O4
10 D3
9 O3

Description

The 'F189 ia a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-State Outputs for Data Bus Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-chip**
- **Diode Clamped Inputs Minimize Ringing**

Logic Symbol


2
4
6
10
12
3
CS
D1
D2
D3
D4
WE
1
A0
15
A1
14
A2
13
A3
O1
O2
O3
O4
5
7
9
11

VCC = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	VCC = +5.0 V ±5%, TA = 0° C to +70° C	VCC = +5.0 V ±10%, TA = -55° C to +125° C	
Plastic DIP (P)	74F189PC		9B
Ceramic DIP (D)	74F189DC	54F189DM	6B
Flatpak (F)		54F189FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

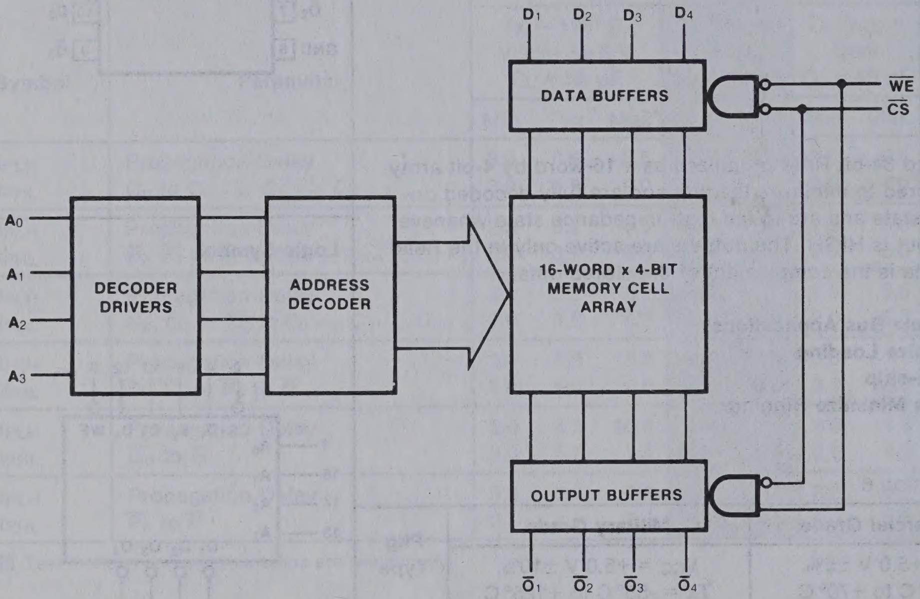
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.75
$D_1 - D_4$	Data Inputs	0.5/0.375
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	25/12.5

Function Table

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



D1
D2
D3
D4
DATA BUFFERS
WE
CS
A0
A1
A2
A3
DECODER DRIVERS
ADDRESS DECODER
16-WORD x 4-BIT MEMORY CELL ARRAY
OUTPUT BUFFERS
Ō1
Ō2
Ō3
Ō4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Access Time, HIGH or LOW	8.0	12	15.5	8.0	22	8.0	18	ns	3-1
t_{PHL}	A_n to $\overline{O}_n$	8.0	12	15.5	8.0	22	8.0	18		3-10
t_{PZH}	Access Time, HIGH or LOW	3.5	5.0	6.5	3.5	9.0	3.5	7.5	ns	3-1, 3-12
t_{PZL}	$\overline{CS}$ to $\overline{O}_n$	5.5	8.0	10	5.5	14	5.5	11.5		3-13
t_{PHZ}	Disable Time, HIGH or LOW	2.0	3.5	4.7	2.5	7.0	2.0	5.5	ns	3-1, 3-12
t_{PLZ}	$\overline{CS}$ to $\overline{O}_n$	2.5	4.2	5.6	2.5	8.0	2.5	6.5		3-13
t_{PZH}	Write Recovery Time, HIGH or LOW	9.0	13.5	17	9.0	24	9.0	19.5	ns	3-1, 3-12
t_{PZL}	$\overline{WE}$ to $\overline{O}_n$	6.5	9.2	12	6.5	17	6.5	14		3-13
t_{PHZ}	Disable Time, HIGH or LOW	3.5	5.0	6.5	3.5	9.0	3.5	7.5	ns	3-1, 3-12
t_{PLZ}	$\overline{WE}$ to $\overline{O}_n$	4.5	6.5	8.5	4.5	12	4.5	9.5		3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	0			0		0		ns	3-16
t_s (L)	A_n to $\overline{WE}$	0			0		0			
t_h (H)	Hold Time, HIGH or LOW	0			0		0			
t_h (L)	A_n to $\overline{WE}$	0			0		0			
t_s (H)	Setup Time, HIGH or LOW	10			10		10		ns	3-14
t_s (L)	D_n to $\overline{WE}$	10			10		10			
t_h (H)	Hold Time, HIGH or LOW	0			0		0			
t_h (L)	D_n to $\overline{WE}$	0			0		0			
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	6.0			6.0		6.0		ns	3-14
t_h (L)	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	0			0		0			
t_w (L)	$\overline{WE}$ Pulse Width LOW	6.0			6.0		6.0		ns	3-16

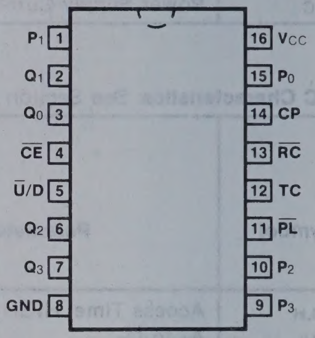
▨ Test limits in screened columns are preliminary.

54F/74F190

Up/Down Decade Counter

(With Preset and Ripple Clock)

Connection Diagram

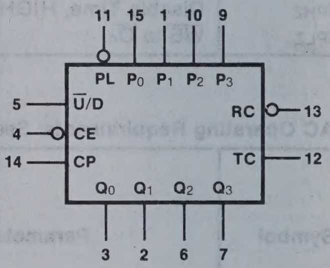


Description

The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **High-speed — 110 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

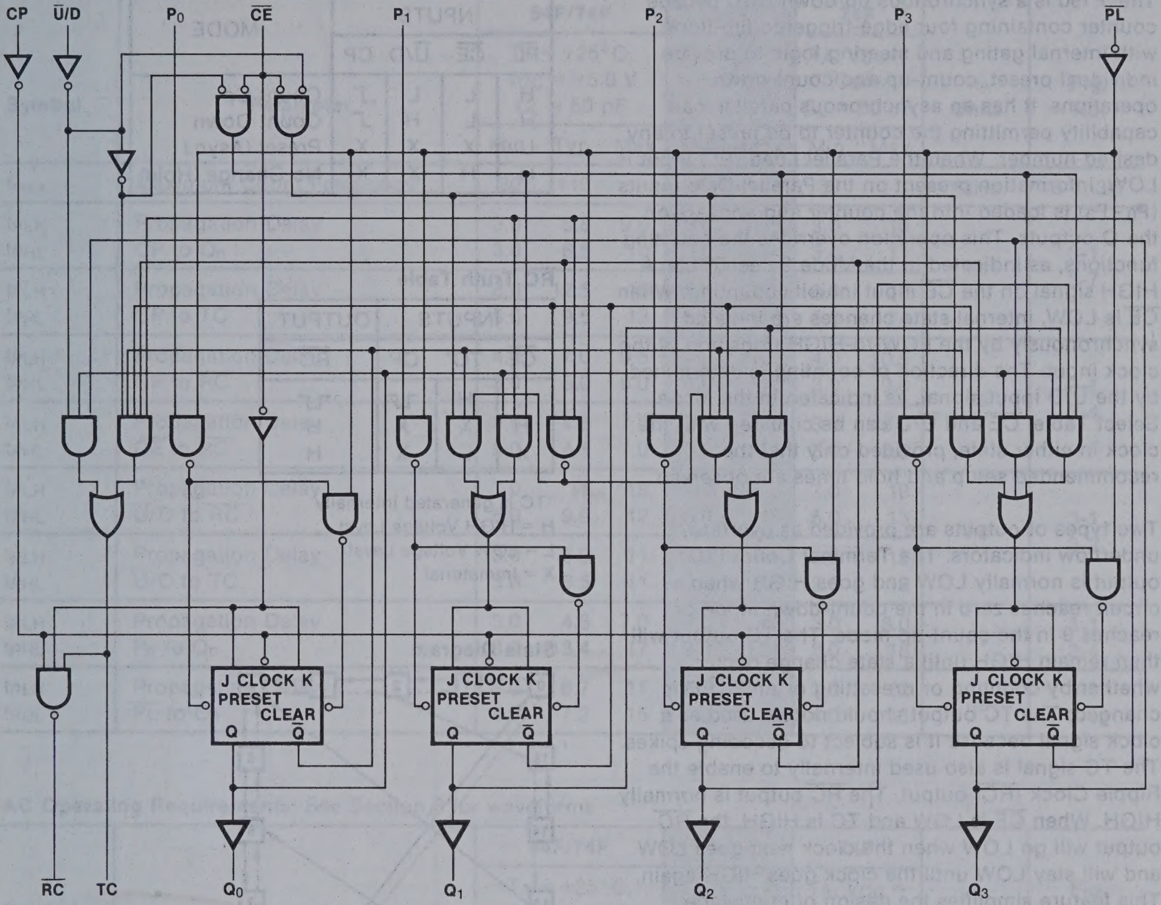
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0$ V ±5%, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0$ V ±10%, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F190PC		9B
Ceramic DIP (D)	74F190DC	54F190DM	7B
Flatpak (F)		54F190FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$P_0 - P_0$	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}/D$	Up/Down Count Control Input	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

Logic Diagram


CP
U/D
P0
CE
P1
P2
P3
PL
J CLOCK K
PRESET
CLEAR
Q
Q
RC
TC
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs ($P_0 - P_3$) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 'F191 data sheet.

Mode Select Table

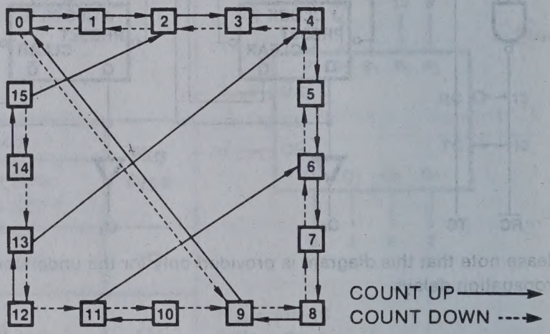
INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	80	110		80		80		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	3.0	5.5	9.0	3.0	12.5	3.0	10	ns	3-1 3-7
t_{PHL}	CP to Q_n	3.0	6.5	10	3.0	14	3.0	11		
t_{PLH}	Propagation Delay	8.0	12.5	16	8.0	22.5	8.0	17		
t_{PHL}	CP to TC	5.0	9.5	13	5.0	18	5.0	14		
t_{PLH}	Propagation Delay	4.0	7.0	9.5	4.0	13.5	4.0	10.5	ns	3-1 3-4
t_{PHL}	CP to $\overline{RC}$	3.0	5.0	8.0	3.0	11	3.0	9.0		
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0		
t_{PHL}	$\overline{CE}$ to $\overline{RC}$	3.0	4.5	7.0	3.0	10	3.0	8.0		
t_{PLH}	Propagation Delay	7.0	11	18	7.0	25.5	7.0	19	ns	3-1 3-2
t_{PHL}	U/$\overline{D}$ to $\overline{RC}$	5.0	9.0	12	5.0	17	5.0	13		
t_{PLH}	Propagation Delay	3.0	6.0	11	3.0	15.5	3.0	12		
t_{PHL}	U/$\overline{D}$ to TC	3.0	6.5	11	3.0	15.5	3.0	12		
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	ns	3-1 3-4
t_{PHL}	P_n to Q_n	8.0	13.4	17	8.0	24	8.0	18		
t_{PLH}	Propagation Delay	3.0	6.7	11	3.0	15.5	3.0	12	ns	3-1 3-11
t_{PHL}	$\overline{PL}$ to Q_n	4.0	7.2	15	4.0	21	4.0	16		

AC Operating Requirements: See Section 3 for waveforms

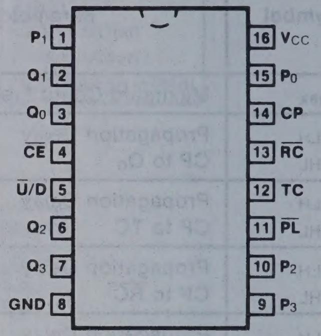
Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0\ V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	5.0			5.0		5.0		ns	3-14
t_s (L)	P_n to $\overline{PL}$	8.0			8.0		8.0			
t_h (H)	Hold Time, HIGH or LOW	3.0			3.0		3.0			
t_h (L)	P_n to $\overline{PL}$	3.0			3.0		3.0			
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	10			10		10		ns	3-5
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0			0		0			
t_w (L)	$\overline{PL}$ Pulse Width LOW	6.0			6.0		6.0		ns	3-11
t_w (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns	3-7
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0			7.0		7.0		ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F191

Up/Down Binary Counter
(With Preset and Ripple Clock)

Connection Diagram

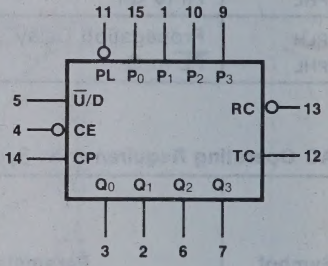


Description

The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **High-Speed — 110 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F191PC		9B
Ceramic DIP (D)	74F191DC	54F191DM	7B
Flatpak (F)		54F191FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}/D$	Up/Down Count Control Input	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

Functional Description

The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs ($P_0 - P_3$) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}/D$ input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}/D$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Mode Select Table

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}/D$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in *Figures a* and *b*. In *Figure a*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

$\overline{RC}$ Truth Table

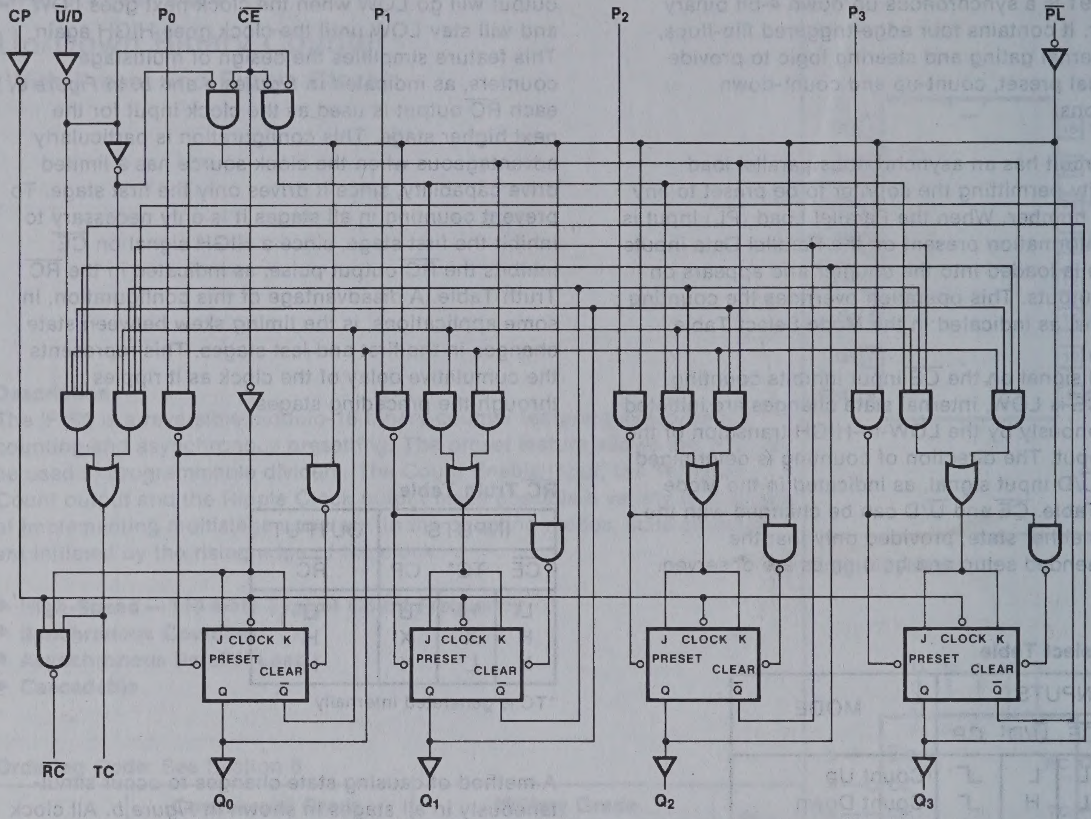
INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

*TC is generated internally

A method of causing state changes to occur simultaneously in all stages in shown in *Figure b*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure c* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures a* and *b* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Logic Diagram


CP
U/D
P0
CE
P1
P2
P3
PL
J CLOCK K
PRESET
CLEAR
Q
Q̄
RC
TC
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fig. a N-Stage Counter Using Ripple Clock

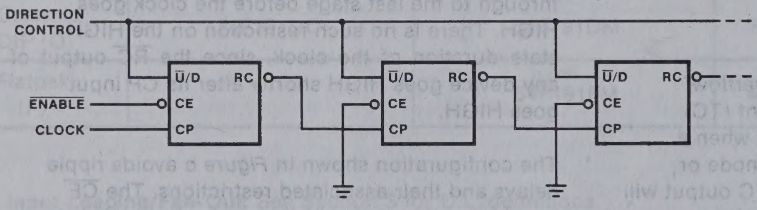

DIRECTION CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP

Fig. b Synchronous N-Stage Counter Using Ripple Carry/Borrow

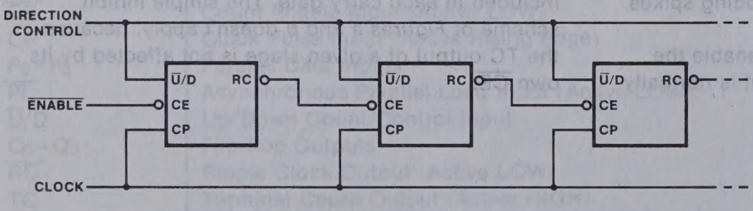
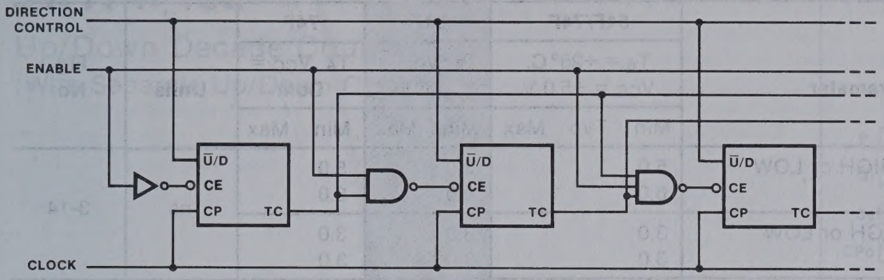

DIRECTION CONTROL
ENABLE
CLOCK
U/D
RC
CE
CP

Fig. c **Synchronous N-Stage Counter with Parallel Gated Carry/Borrow**



DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Maximum Count Frequency	80	110		80		80		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	3.0	5.5	9.0	3.0	12.5	3.0	10	ns	3-1 3-7
t_{PHL}	CP to Q_n	3.0	6.5	10	3.0	14	3.0	11		
t_{PLH}	Propagation Delay	8.0	12.5	16	8.0	22.5	8.0	17		
t_{PHL}	CP to TC	5.0	9.5	13	5.0	18	5.0	14		
t_{PLH}	Propagation Delay	4.0	7.0	9.5	4.0	13.5	4.0	10.5	ns	3-1 3-4
t_{PHL}	CP to $\overline{RC}$	3.0	5.0	8.0	3.0	11	3.0	9.0		
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0		
t_{PHL}	$\overline{CE}$ to $\overline{RC}$	3.0	4.5	7.0	3.0	10	3.0	8.0		
t_{PLH}	Propagation Delay	7.0	11	18	7.0	25.5	7.0	19	ns	3-1 3-2
t_{PHL}	$\overline{U}$/D to $\overline{RC}$	5.0	9.0	12	5.0	17	5.0	13		
t_{PLH}	Propagation Delay	3.0	6.0	11	3.0	15.5	3.0	12		
t_{PHL}	$\overline{U}$/D to TC	3.0	6.5	11	3.0	15.5	3.0	12		
t_{PLH}	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	ns	3-1 3-4
t_{PHL}	P_n to Q_n	8.0	13.4	17	8.0	24	8.0	18		
t_{PLH}	Propagation Delay	3.0	6.7	11	3.0	15.5	3.0	12	ns	3-1 3-11
t_{PHL}	$\overline{PL}$ to Q_n	4.0	7.2	15	4.0	21	4.0	16		

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0 8.0			5.0 8.0		5.0 8.0		ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0			3.0 3.0		3.0 3.0			
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	10			10		10		ns	3-5
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0			0		0			
t_w (L)	$\overline{PL}$ Pulse Width, LOW	6.0			6.0		6.0		ns	3-11
t_w (L)	CP Pulse Width, LOW	6.0			6.0		6.0		ns	3-7
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0			7.0		7.0		ns	3-11

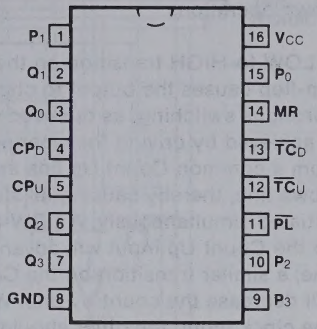
▨ Test limits in screened columns are preliminary.

54F/74F192

Up/Down Decade Counter

(With Separate Up/Down Clocks)

Connection Diagram

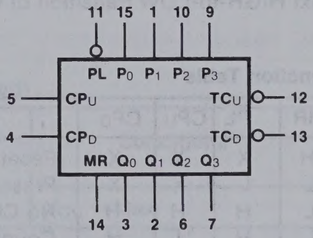


Description

The 'F192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0\ V \pm 10\%$, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F192PC		9B
Ceramic DIP (D)	74F192DC	54F192DM	6B
Flatpak (F)		54F192FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/0.75
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/0.75
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{TC_D}$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC_U}$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

Functional Description

The 'F192 is an asynchronously presettable decade counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally HIGH. When the circuit has reached the maximum count state 9, the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays, Similarly, the $\overline{TC_D}$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC_U} = Q_0 \bullet Q_3 \bullet \overline{CP_U}$$
$$\overline{TC_D} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$$

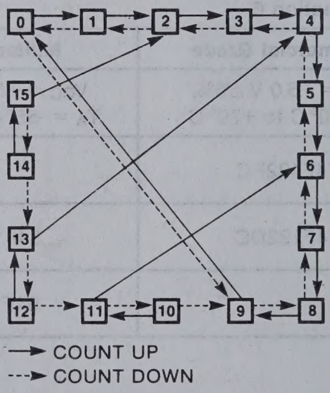
The 'F192 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input ($P_0 - P_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

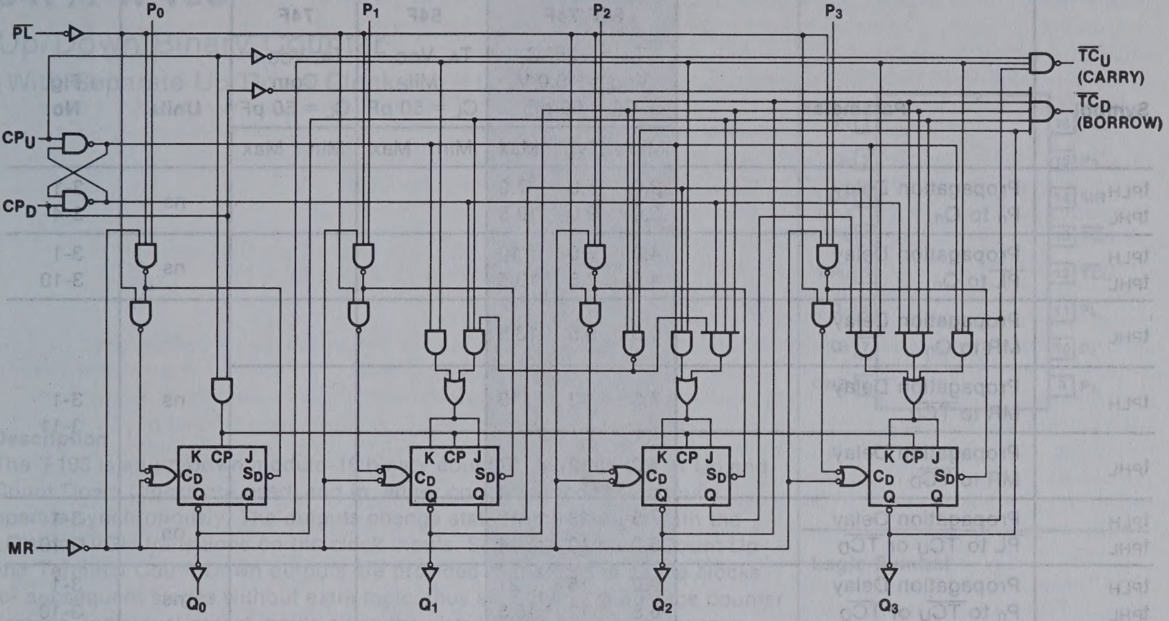
MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



$\overline{PL}$
P0
P1
P2
P3
$\overline{TC}_U$ (CARRY)
$\overline{TC}_D$ (BORROW)
CPU
CPD
K CP J
CD
SD
Q
MR
Q0
Q1
Q2
Q3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	80							MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$	3.0 3.0	6.5 6.5	9.0 9.0					ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	5.0 3.5	9.0 6.0	13 8.5					ns	3-1 3-7

▨ Test limits in screened columns are preliminary.

AC Characteristics (Cont'd): See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay P_n to Q_n	3.0	5.0	7.0					ns	3-1
t_{PHL}		5.0	9.0	12.5						3-4
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	4.0	7.0	10					ns	3-1
t_{PHL}		4.5	7.5	10.5						3-10
t_{PHL}	Propagation Delay MR to Q_n	5.5	9.5	13.5						
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	7.5	13	18					ns	3-1 3-11
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	7.0	12	17						
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.5	13	18					ns	3-1
t_{PHL}		6.0	10	14						3-10
t_{PLH}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	9.0	15	21					ns	3-1
t_{PHL}		6.5	11	15.5						3-10

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0							ns	3-14
t_s (L)		8.0								
t_h (H)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0								
t_h (L)		3.0								
t_w (L)	$\overline{PL}$ Pulse Width LOW	12							ns	3-11
t_w (L)	CP_U or CP_D Pulse Width LOW	8.0							ns	3-7
t_w (H)	MR Pulse Width HIGH	8.0							ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	10							ns	3-11
t_{rec}	Recovery Time MR to CP_U or CP_D	6.0							ns	3-11

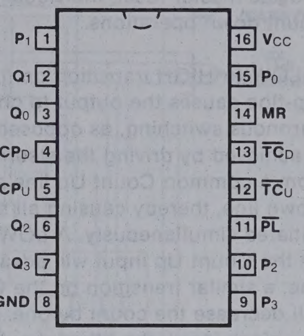
▨ Test limits in screened columns are preliminary.

54F/74F193

Up/Down Binary Counter

(With Separate Up/Down Clocks)

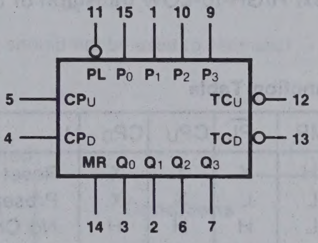
Connection Diagram



Description

The 'F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0°C$ to $+70°C$	Military Grade $V_{CC} = +5.0\ V \pm 10\%$, $T_A = -55°C$ to $+125°C$	Pkg Type
Plastic DIP (P)	74F193PC		9B
Ceramic DIP (D)	74F193DC	54F193DM	6B
Flatpak (F)		54F193FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/0.75
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/0.75
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

Function Description

The 'F193 is a 4-bit binary synchronous up/down (reversible) counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally HIGH. When the circuit has reached the maximum count state 15, the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC_D}$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC_U} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP_U}$$
$$\overline{TC_D} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$$

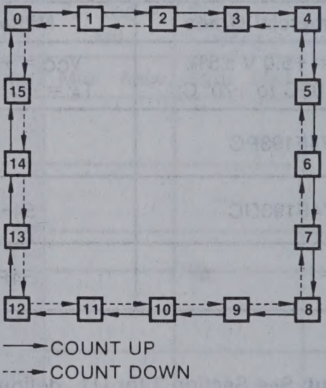
The 'F193 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input ($P_0 - P_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

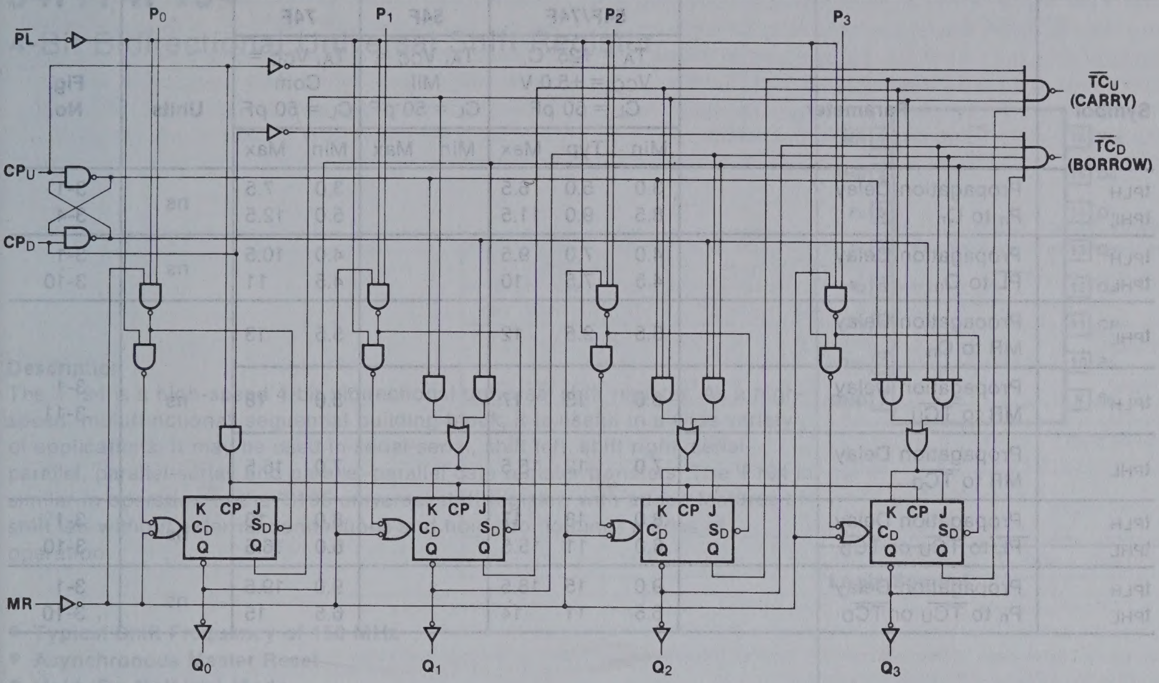
MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	_|‾	H	Count Up
L	H	H	_|‾	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	80					80		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	5.0	9.0	11.5			5.0	12.5	ns	3-1
t_{PHL}	CP_U or CP_D to $\overline{TC}_U$	3.5	6.0	8.0			3.5	9.0		3-4
t_{PLH}	Propagation Delay	3.0	6.5	9.5			3.0	10.5	ns	3-1
t_{PHL}	CP_U or CP_D to Q_n	3.0	6.5	9.5			3.0	10.5		3-7

AC Characteristics (Cont'd): See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 8.5	5.0 9.0	6.5 11.5			3.0 5.0	7.5 12.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	4.0 4.5	7.0 7.5	9.5 10			4.0 4.5	10.5 11	ns	3-1 3-10
t_{PHL}	Propagation Delay MR to Q_n	5.5	9.5	12			5.5	13	ns	3-1 3-11
t_{PLH}	Propagation Delay MR to $\overline{TC_U}$	8.0	13	17			8.0	18		
t_{PHL}	Propagation Delay MR to $\overline{TC_D}$	7.0	12	15.5			7.0	16.5		
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$	8.0 6.0	13 11	17 15.5			8.0 6.0	18 16.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC_U}$ or $\overline{TC_D}$	9.0 6.5	15 11	18.5 14			9.0 6.5	19.5 15	ns	3-1 3-10

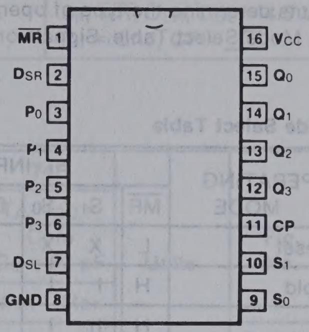
AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0 8.0					5.0 8.0		ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0					3.0 3.0			
t_w (L)	$\overline{PL}$ Pulse Width LOW	12					12		ns	3-11
t_w (L)	CP_U or CP_D Pulse Width LOW	8.0					8.0		ns	3-7
t_w (H)	MR Pulse Width HIGH	8.0					8.0		ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	10					10		ns	3-11
t_{rec}	Recovery Time MR to CP_U or CP_D	6.0					6.0		ns	3-11

54F/74F194

4-Bit Bidirectional Universal Shift Register

Connection Diagram

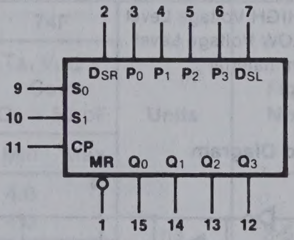


Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- **Typical Shift Frequency of 150 MHz**
- **Asynchronous Master Reset**
- **Hold (Do Nothing) Mode**
- **Fully Synchronous Serial or Parallel Data Transfers**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F194PC		9B
Ceramic DIP (D)	74F194DC	54F194DM	6B
Flatpak (F)		54F194FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
D_{SR}	Serial Data Input (Shift Right)	0.5/0.375
D_{SL}	Serial Data Input (Shift Left)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$Q_0 - Q_3$	Parallel Outputs	25/12.5

Functional Description

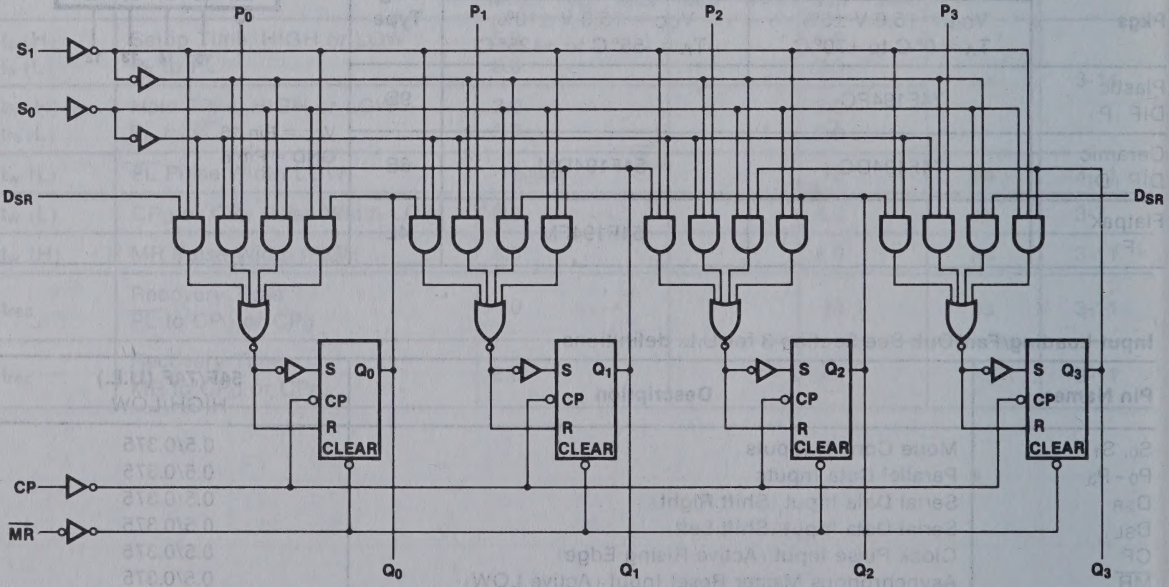
The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data ($P_0 - P_3$) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

Mode Select Table

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
Shift Right	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	46	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = 4.5 V P_n = Gnd, CP = _┌

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	105	150		90		90		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns	3-1
t_{PHL}	CP to Q_n	3.5	5.5	7.0	3.0	8.5	3.5	8.0		3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	8.6	12	4.5	14.5	4.5	14	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

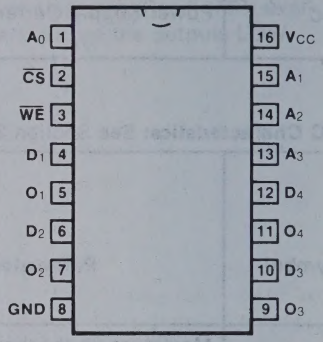
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	4.0			4.0		4.0		ns	3-5
t_s (L)	P_n or D_{SR} or D_{SL} to CP	4.0			4.0		4.0			
t_h (H)	Hold Time, HIGH or LOW	0			1.0		1.0			
t_h (L)	P_n or D_{SR} or D_{SL} to CP	0			1.0		1.0			
t_s (H)	Setup Time, HIGH or LOW	8.0			9.5		9.0		ns	3-5
t_s (L)	S_n to CP	8.0			8.0		8.0			
t_h (H)	Hold Time, HIGH or LOW	0			0		0			
t_h (L)	S_n to CP	0			0		0			
t_w (H)	CP Pulse Width HIGH	5.0			5.5		5.5		ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0			9.0		8.0		ns	3-11

54F/74F219

64-Bit Random Access Memory

(With 3-State Outputs)

Connection Diagram

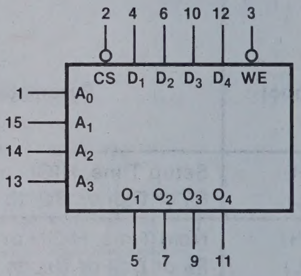


Description

The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

- **3-State Outputs for Data Bus Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-chip**
- **Diode Clamped Inputs Minimize Ringing**

Logic Symbol



VCC = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	VCC = +5.0 V ±5%, TA = 0° C to +70° C	VCC = +5.0 V ±10%, TA = -55° C to +125° C	
Plastic DIP (P)	74F219PC		9B
Ceramic DIP (D)	74F219DC	54F219DM	6B
Flatpak (F)		54F219FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

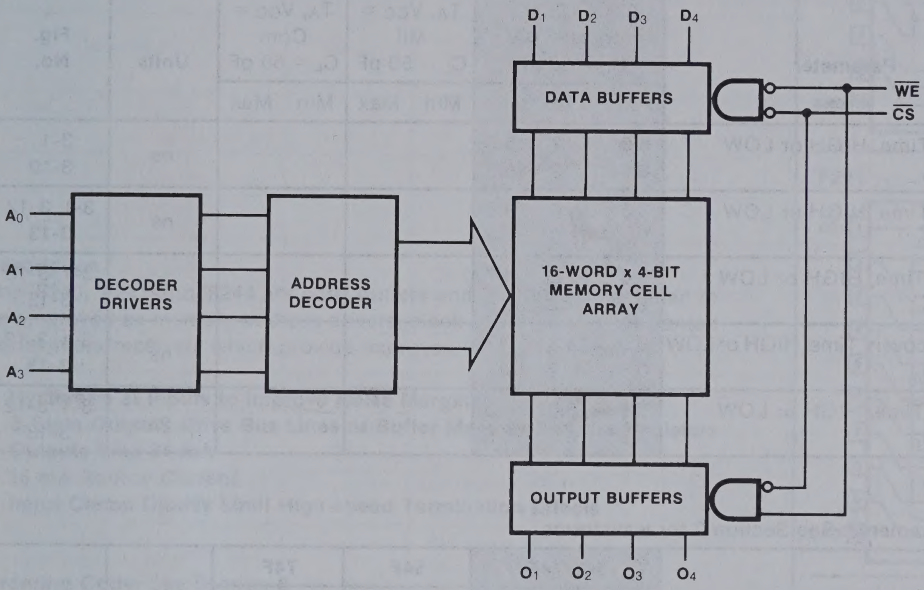
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
A0 - A3	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.75
D1 - D4	Data Inputs	0.5/0.375
O1 - O4	3-State Data Outputs	25/12.5

Function Table

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


D1
D2
D3
D4
DATA BUFFERS
WE
CS
A0
A1
A2
A3
DECODER DRIVERS
ADDRESS DECODER
16-WORD x 4-BIT MEMORY CELL ARRAY
OUTPUT BUFFERS
O1
O2
O3
O4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to O_n	8.0 8.0	12 12	15.5 15.5					ns	3-1 3-10
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{CS}$ to O_n	3.5 5.5	5.0 8.0	6.5 10					ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{CS}$ to O_n	2.0 2.5	3.5 4.2	4.7 5.6					ns	3-1, 3-12 3-13
t_{PZH} t_{PZL}	Write Recovery Time, HIGH or LOW $\overline{WE}$ to O_n	9.0 6.5	13.5 9.2	17 12					ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{WE}$ to O_n	3.5 4.5	5.0 6.5	6.5 8.5					ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0							ns	3-16
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	10 10							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0								
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	6.0							ns	3-14
t_h (L)	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	0							ns	3-14
t_w (L)	$\overline{WE}$ Pulse Width LOW	6.0							ns	3-16

▨ Test limits in screened columns are preliminary.

54F/74F240 • 54F/74F241 • 54F/74F244

Octal Buffer/Line Driver

(With 3-State Outputs)

Description

The 'F240, 'F241 and 'F244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

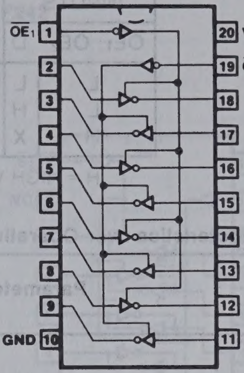
- **Hysteresis at Inputs to Improve Noise Margins**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Sink 64 mA**
- **15 mA Source Current**
- **Input Clamp Diodes Limit High-speed Termination Effects**

Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F240PC, 74F241PC 74F244PC		9Z
Ceramic DIP (D)	74F240DC, 74F241DC 74F244DC	54F240DM, 54F241DM 54F244DM	4E
Flatpak (F)		54F240FM, 54F241FM 54F244FM	4D

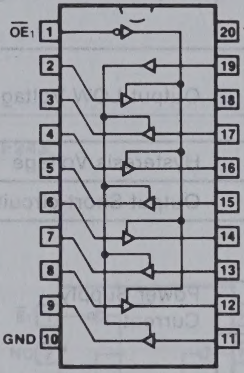
Connection Diagrams

'F240



OE1
1
2
3
4
5
6
7
8
9
GND
10
20
VCC
19
OE2
18
17
16
15
14
13
12
11

'F241



OE1
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GND
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VCC
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OE2
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16
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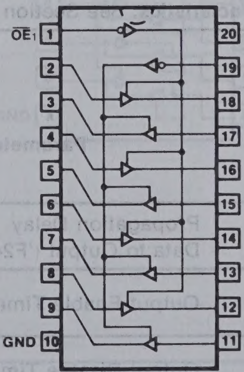
14
13
12
11

'F244



OE1
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6
7
8
9
GND
10
20
VCC
19
OE2
18
17
16
15
14
13
12
11

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Input (Active LOW)	0.5/0.625
OE_2	3-State Output Enable Input (Active HIGH)	0.5/0.625
	Inputs ('F240)	0.5/0.625*
	Inputs ('F241, 'F244)	0.5/1.0*
	Outputs	75/40 (30)

*Worst-case ('F240 enabled; 'F241, 'F244 disabled)

Truth Tables

'F240

INPUTS		OUTPUT
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

'F241

INPUTS			OUTPUT
$\overline{OE}_1$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

'F244

INPUTS		OUTPUT
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions	
			Min	Typ	Max			
V_{OH}	Output HIGH Voltage	XM, XC	2.4			V	I_{OH} = -3.0 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	
		XM	2.0			V	I_{OH} = -12 mA	V_{IH} = 2.0 V V_{CC} = Min V_{IL} = 0.5 V
		XC	2.0				I_{OH} = -15 mA	
V_{OL}	Output LOW Voltage	XM			0.55	V	I_{OL} = 48 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min
		XC			0.55		I_{OL} = 64 mA	
$V_{T+} - V_{T-}$	Hysteresis Voltage		0.2	0.4		V	V_{CC} = Min	
I_{OS}	Output Short-circuit Current		-100		-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CCH}	Power Supply Current	'F240		19	29	mA	Outputs HIGH	V_{CC} = Max
		'F241, 'F244		40	60			
I_{CCL}		'F240		50	75	mA	Outputs LOW	
		'F241, 'F244		60	90			
I_{CCZ}		'F240		42	63	mA	Outputs OFF	
		'F241, 'F244		60	90			

AC Characteristics: See Section 3 for waveforms and load configurations

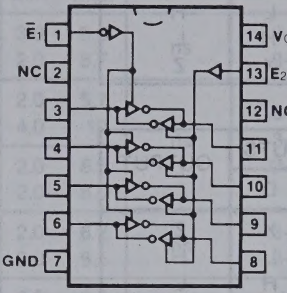
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F240)	3.0 2.0	5.1 3.5	7.0 4.7	3.0 2.0	9.0 6.0	3.0 2.0	8.0 5.7	ns	3-1 3-3
t_{PZH} t_{PZL}	Output Enable Time ('F240)	2.0 4.0	3.5 6.9	4.7 9.0	2.0 4.0	6.5 10.5	2.0 4.0	5.7 10	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F240)	2.0 2.0	4.0 6.0	5.3 8.0	2.0 2.0	6.5 12.5	2.0 2.0	6.3 9.5		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F241, 'F244)	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.5 7.0	2.5 2.5	6.2 6.5	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time ('F241, 'F244)	2.0 2.0	4.3 5.4	5.7 7.0	2.0 2.0	7.0 8.5	2.0 2.0	6.7 8.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F241, 'F244)	2.0 2.0	4.5 4.5	6.0 6.0	2.0 2.0	7.0 7.5	2.0 2.0	7.0 7.0		

54F/74F242 • 54F/74F243

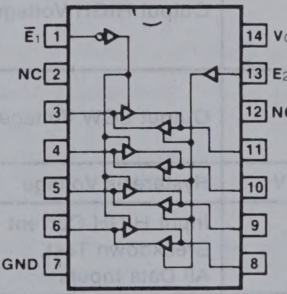
Quad Bus Transceiver
(With 3-State Outputs)

Connection Diagrams

'F242



'F243



Description

The 'F242 and 'F243 are quad bus transmitters/receivers designed for 4-line asynchronous 2-way data communications between data busses.

- **Hysteresis at Inputs to Improve Noise Immunity**
- **2-Way Asynchronous Data Bus Communication**
- **Input Clamp Diodes Limit High-speed Termination Effects**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F242PC, 74F243PC		9A
Ceramic DIP (D)	74F242DC, 74F243DC	54F242DM, 54F243DM	6A
Flatpak (F)		54F242FM, 54F243FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.625
E_2	Enable Input (Active HIGH)	0.5/0.625
	Inputs ('F242)	1.75/0.625*
	Inputs ('F243)	1.75/1.0*
	Outputs	75/40 (30)

*Worst-case ('F242 enabled, 'F243 disabled)

Truth Tables

'F242

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	H
L	H	L
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
H	L	H
H	H	L

'F243

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
H	L	L
H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	XM, XC	2.4			V	I_{OH} = -3.0 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	
		XM	2.0			V	I_{OH} = -12 mA	V_{IH} = 2.0 V V_{CC} = Min V_{IL} = 0.5 V
		XC	2.0				I_{OH} = -15 mA	
V_{OL}	Output LOW Voltage	XM			0.55	V	I_{OL} = 48 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min
		XC			0.55		I_{OL} = 64 mA	
$V_{T+} - V_{T-}$	Hysteresis Voltage		0.2	0.4		V	V_{CC} = Min	
I_{IH}	Input HIGH Current Breakdown Test, All Data Inputs				100	μA	V_{OUT} = 5.5 V, V_{CC} = Max	
I_{OZH}	Output OFF Current HIGH				70	μA	V_{OUT} = 2.7 V	V_{IN} = V_{IH} or V_{IL} V_{CC} = Max
					100		V_{OUT} = 5.5 V	
I_{OZL}	Output OFF Current LOW				-1.6	mA	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0.4 V	
I_{OS}	Output Short-circuit Current		-100		-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CCH}	Power Supply Current	'F242		30	46	mA	Outputs HIGH	V_{CC} = Max
		'F243		64	80			
I_{CCL}		'F242		46	69	mA	Outputs LOW	
		'F243		64	90			
I_{CCZ}		'F242		42	63	mA	Outputs OFF	
		'F243		71	90			

AC Characteristics: See Section 3 for waveforms and load configurations

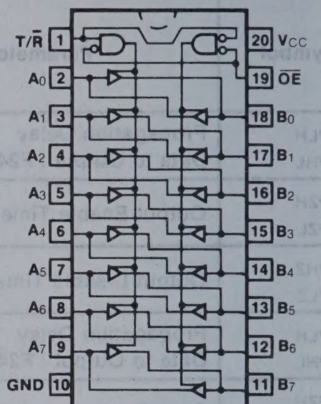
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output ('F242)	3.0	5.1	7.0			3.0	8.0	ns	3-1
t_{PHL}		2.0	3.5	4.7			2.0	5.7		3-3
t_{PZH}	Output Enable Time ('F242)	2.0	3.5	4.7			2.0	5.7	ns	3-1 3-12 3-13
t_{PZL}		4.0	6.9	9.0			4.0	10		
t_{PHZ}	Output Disable Time ('F242)	2.0	4.0	5.3			2.0	6.3		
t_{PLZ}		2.0	3.9	6.5			2.0	8.0		
t_{PLH}	Propagation Delay Data to Output ('F243)	2.5	4.0	5.2	2.0	6.5	2.0	6.2	ns	3-1
t_{PHL}		2.5	4.0	5.2	2.0	8.5	2.0	6.5		3-4
t_{PZH}	Output Enable Time ('F243)	2.0	4.3	5.7	2.0	8.0	2.0	6.7	ns	3-1 3-12 3-13
t_{PZL}		2.0	5.8	7.5	2.0	10.5	2.0	8.5		
t_{PHZ}	Output Disable Time ('F243)	2.0	4.5	6.0	2.0	7.5	2.0	7.0		
t_{PLZ}		2.0	4.5	6.0	2.0	8.5	2.0	7.0		

54F/74F245

Octal Bidirectional Transceiver

(With 3-State Inputs/Outputs)

Connection Diagram



Description

The 'F245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The transmit/ Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-Z condition.

- **Non-Inverting Buffers**
- **Bidirectional Data Path**
- **B Outputs Sink 64 mA**
- **Hysteresis on A and B Inputs**
- **MOS Compatible**

Truth Table

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F245PC		9Z
Ceramic DIP (D)	74F245DC	54F245DM	4E
Flatpak (F)		54F245FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/1.0
T/$\overline{R}$	Transmit/Receive Input	0.5/0.5
A_0 - A_7	Side A 3-State Inputs or 3-State Outputs	1.75/0.625* 25/12.5
B_0 - B_7	Side B 3-State Inputs or 3-State Outputs	1.75/0.625* 25/40 (30)

*Worst-case (disabled)

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions	
			Min	Typ	Max			
V_{OH}	Output HIGH Voltage $B_0 - B_7$	XM	2.0			V	$I_{OH} = -12$ mA	V_{CC} = Min
		XC	2.0				$I_{OH} = -15$ mA	
	Output HIGH Voltage $B_0 - B_7$		2.4			V	$I_{OH} = -3.0$ mA	
V_{OL}	Output LOW Voltage $B_0 - B_7$	XM			0.55	V	$I_{OL} = 48$ mA	V_{CC} = Min
		XC			0.55		$I_{OL} = 64$ mA	
$V_{T+} - V_{T-}$	Hysteresis Voltage $B_0 - B_7$		200	400		mV	V_{CC} = Min	
I_{IH}	Input HIGH Current Breakdown Test — A_n, B_n				1.0	mA	V_{CC} = Max, $V_{IN} = 5.5$ V	
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH — A_n, B_n				70	µA	V_{CC} = Max, $V_{OUT} = 2.4$ V	
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW — A_n, B_n				1.0	mA	V_{CC} = Max, $V_{OUT} = 0.5$ V	
I_{OS}	Output Short-circuit Current $B_0 - B_7$		-100		-225	mA	V_{CC} = Max, $V_{OUT} = 0$ V	
I_{CC}	Power Supply Current			95	143	mA	V_{CC} = Max	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			T_A, V_{CC} = Mil, $C_L = 50$ pF		T_A, V_{CC} = Com, $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay An to Bn or Bn to An	2.5	4.2	5.5			2.5	6.5	ns	3-1
t_{PHL}		2.5	4.6	6.0			2.5	7.0		3-4
t_{PZH}	Output Enable Time	3.0	5.3	7.0			3.0	8.0	ns	3-1
t_{PZL}		4.5	7.9	10			4.5	11		3-12
t_{PHZ}	Output Disable Time	3.0	5.0	6.5			3.0	7.5		3-13
t_{PLZ}		2.0	3.7	5.0			2.0	6.0		

54F/74F251

8-Input Multiplexer

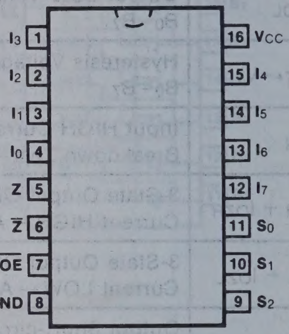
(With 3-State Outputs)

Description

The 'F251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **Multifunctional Capability**
- **On-chip Select Logic Decoding**
- **Inverting and Non-inverting 3-State Outputs**

Connection Diagram


I_3 1
I_2 2
I_1 3
I_0 4
Z 5
$\overline{Z}$ 6
$\overline{OE}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2

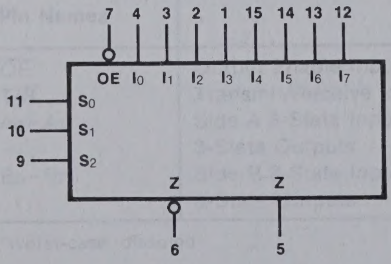
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F251PC		9B
Ceramic DIP (D)	74F251DC	54F251DM	6B
Flatpak (F)		54F251FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$I_0 - I_7$	Multiplexer Inputs	0.5/0.375
Z	3-State Multiplexer Output	25/12.5
$\overline{Z}$	Complementary 3-State Multiplexer Output	25/12.5

Logic Symbol


7
4
3
2
1
15
14
13
12
OE
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
11
10
9
S_0
S_1
S_2
$\overline{Z}$
Z
6
5

V_{CC} = Pin 16
GND = Pin 8

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S_0} \bullet \overline{S_1} \bullet \overline{S_2} + I_1 \bullet S_0 \bullet \overline{S_1} \bullet \overline{S_2} + I_2 \bullet \overline{S_0} \bullet S_1 \bullet \overline{S_2} + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S_2} + I_4 \bullet \overline{S_0} \bullet \overline{S_1} \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S_1} \bullet S_2 + I_6 \bullet \overline{S_0} \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

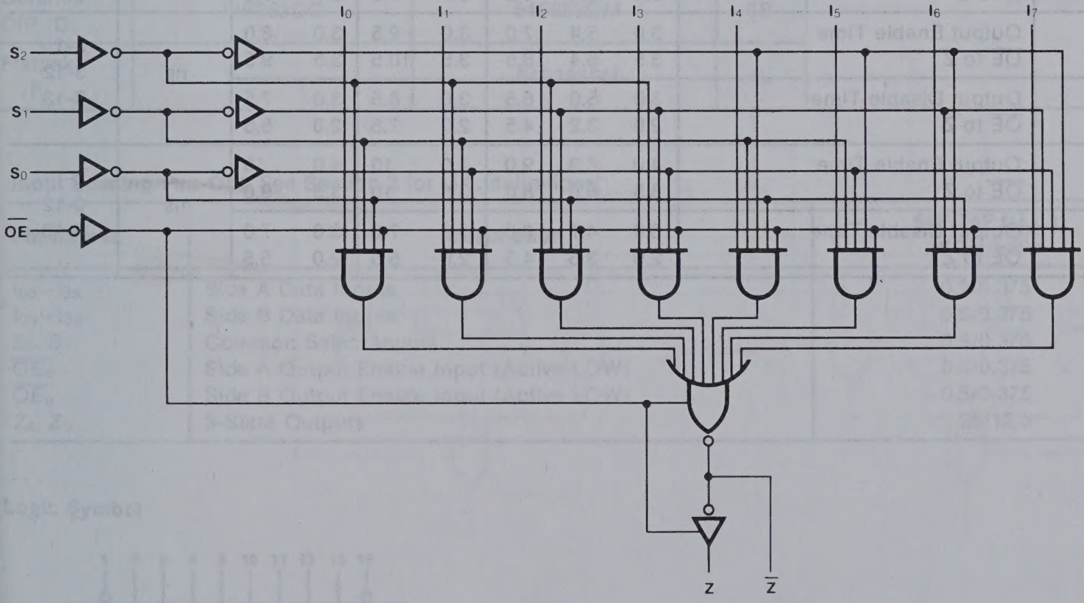
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

INPUTS				OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions	
			Min	Typ	Max			
I_{CC}	Power Supply Current	ON		15	22	mA	I_n, S_n = 4.5 V $\overline{OE}$ = Gnd	V_{CC} = Max
		OFF		16	24		$\overline{OE}$, I_n = 4.5 V	

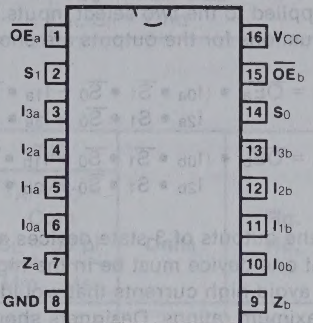
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	4.0 3.2	5.9 5.7	8.0 7.5	3.5 3.2	9.5 9.5	4.0 3.2	9.0 8.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 5.0	9.6 6.9	13 9.0	3.5 3.0	16.5 10.5	4.5 4.0	14 10	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	3.0 2.0	4.1 3.0	5.7 4.0	2.5 2.0	8.0 6.0	3.0 2.0	7.0 5.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	5.5 3.7	7.2 5.1	9.5 6.5	3.5 3.7	11.5 7.5	5.5 3.7	10.5 7.5	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$	3.0 3.5	5.4 6.4	7.0 8.5	3.0 3.5	9.5 10.5	3.0 3.5	8.0 9.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{Z}$	3.0 2.0	5.0 3.2	6.5 4.5	3.0 2.0	8.5 7.5	3.0 2.0	7.5 5.5		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z	4.0 3.5	6.9 6.0	9.0 8.0	4.0 3.5	10 10	4.0 3.5	10 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z	3.0 2.0	4.7 3.5	6.0 4.5	3.0 2.0	7.0 5.5	3.0 2.0	7.0 5.5		

54F/74F253

Dual 4-Input Multiplexer
(With 3-State Outputs)

Connection Diagram


$\overline{OE}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
Z_a 7
GND 8
16 V_{CC}
15 $\overline{OE}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 Z_b

Description

The 'F253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- **FAST Process for High Speed**
- **Multifunction Capability**
- **Non-inverting 3-State Outputs**

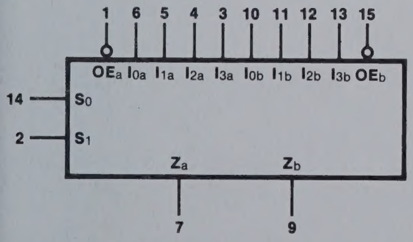
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F253PC		9B
Ceramic DIP (D)	74F253DC	54F253DM	6B
Flatpak (F)		54F253FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
I_{0a} - I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} - I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
Z_a, Z_b	3-State Outputs	25/12.5

Logic Symbol


1
6
5
4
3
10
11
12
13
15
OE_a
I_{0a}
I_{1a}
I_{2a}
I_{3a}
I_{0b}
I_{1b}
I_{2b}
I_{3b}
OE_b
14
S_0
2
S_1
Z_a
Z_b
7
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high-impedance (high-Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE_a} \bullet (I_{0a} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1a} \bullet \overline{S_1} \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S_0} + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE_b} \bullet (I_{0b} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1b} \bullet \overline{S_1} \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S_0} + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high-impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

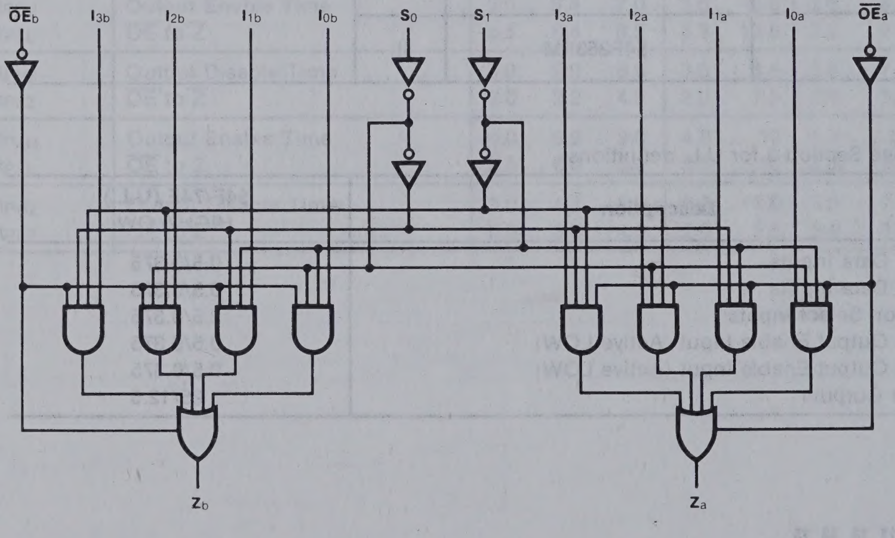
Truth Table

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		11.5	16	mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_0, S_n = 4.5 V; $I_1 - I_3$ = Gnd
I_{CCL}			16	23		V_{CC} = Max I_n, S_n, OE_n = Gnd
I_{CCZ}			16	23		V_{CC} = Max, $\overline{OE}_n$ = 4.5 V I_n, S_n = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	5.5 4.5	10.1 9.2	12.5 11	3.5 2.5	15 12	4.5 3.5	13.5 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0 3.0	5.5 5.5	7.0 7.0	2.5 2.5	9.0 8.0	3.0 3.0	8.0 8.0	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.8 7.2	9.0 9.5	2.5 2.5	10.5 11	3.0 3.0	10 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 9.0	2.0 2.0	6.0 7.0		

▨ Test limits in screened columns are preliminary.

54F/74F257

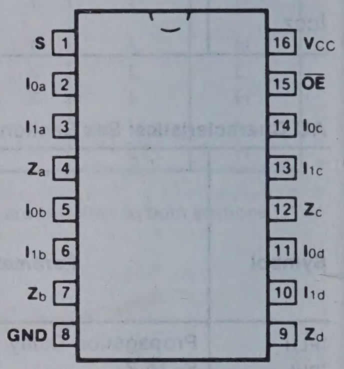
Quad 2-Input Multiplexer
(With 3-State Outputs)

Description

The 'F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- **Multiplexer Expansion by Tying Outputs Together**
- **Non-inverting 3-State Outputs**
- **Input Clamp Diodes Limit High-speed Termination Effects**

Connection Diagram



S 1
I_{0a} 2
I_{1a} 3
Z_a 4
I_{0b} 5
I_{1b} 6
Z_b 7
GND 8
16 V_{CC}
15 $\overline{OE}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

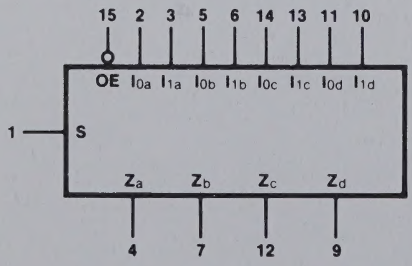
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F257PC		9B
Ceramic DIP (D)	74F257DC	54F257DM	6B
Flatpak (F)		54F257FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
I_{0a} - I_{0d}	Data Inputs from Source 0	0.5/0.375
I_{1a} - I_{1d}	Data Inputs from Source 1	0.5/0.375
Z_a - Z_d	3-State Multiplexer Outputs	25/12.5

Logic Symbol



15
2
3
5
6
14
13
11
10
OE
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
1
S
Z_a
Z_b
Z_c
Z_d
4
7
12
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

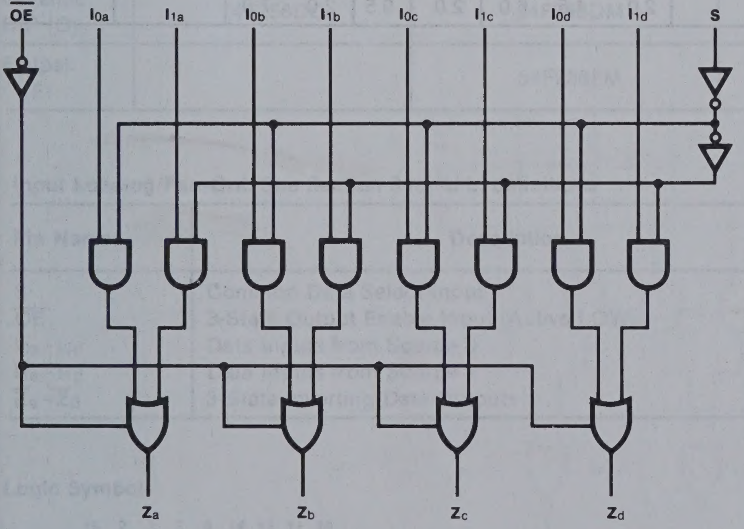
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions
			Min	Typ	Max		
I_{CC}	Power Supply Current	HIGH		9.0	15	mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
		LOW		14.5	22		V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
		OFF		15	23		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

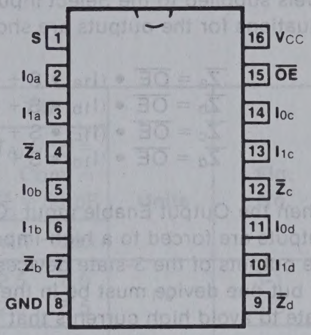
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to Z_n	3.0	4.5	6.0	3.0	8.0	3.0	7.0	ns	3-1
t_{PHL}		2.5	4.2	5.5	2.5	8.0	2.5	6.5		3-4
t_{PLH}	Propagation Delay S to Z_n	4.5	10.1	13	4.5	15.5	4.5	15	ns	3-1
t_{PHL}		3.5	6.5	8.5	3.5	10.5	3.5	9.5		3-10
t_{PZH}	Output Enable Time	3.0	5.9	7.5	3.0	9.5	3.0	8.5	ns	3-1 3-12 3-13
t_{PZL}		3.0	5.5	7.5	3.0	10	3.0	8.5		
t_{PHZ}	Output Disable Time	2.0	4.3	6.0	2.0	7.0	2.0	7.0		
t_{PLZ}		2.0	4.5	6.0	2.0	9.5	2.0	7.0		

54F/74F258

Quad 2-Input Multiplexer

(With 3-State Outputs)

Connection Diagram


S 1
I0a 2
I1a 3
Z̄a 4
I0b 5
I1b 6
Z̄b 7
GND 8
9 Z̄d
10 I1d
11 I0d
12 Z̄c
13 I1c
14 I0c
15 OE
16 VCC

Description

The 'F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high-impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- **Multiplexer Expansion by Tying Outputs Together**
- **Inverting 3-State outputs**

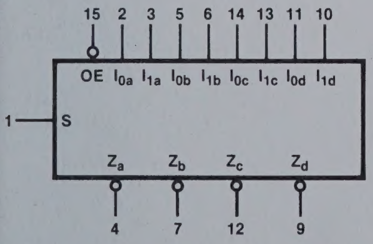
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F258PC		9B
Ceramic DIP (D)	74F258DC	54F258DM	6B
Flatpak (F)		54F258FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$I_{0a}-I_{0d}$	Data Inputs from Source 0	0.5/0.375
$I_{1a}-I_{1d}$	Data Inputs from Source 1	0.5/0.375
$\overline{Z}_a-\overline{Z}_d$	3-State Inverting Data Outputs	25/12.5

Logic Symbol


15
2
3
5
6
14
13
11
10
OE
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
Za
Zb
Zc
Zd
4
7
12
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z_a} = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z_b} = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z_c} = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z_d} = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

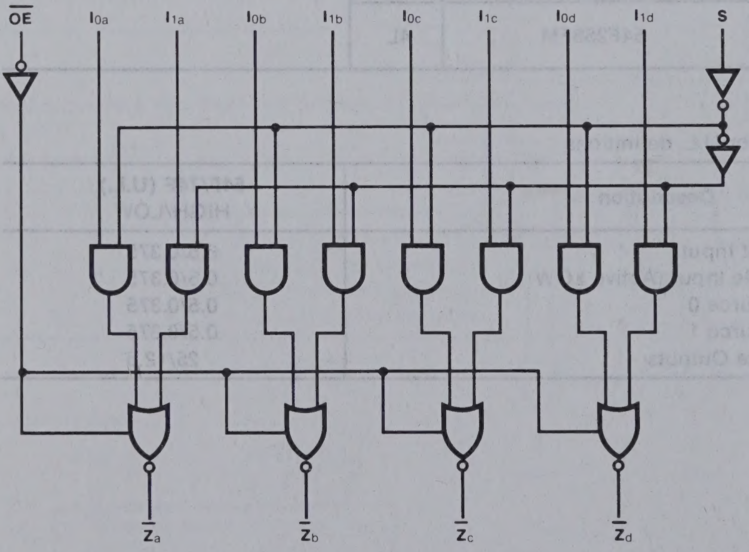
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high-impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CCH}	Power Supply Current		6.2	9.5	mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
I_{CCL}			15.1	23		V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
I_{CCZ}			11.3	17		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V

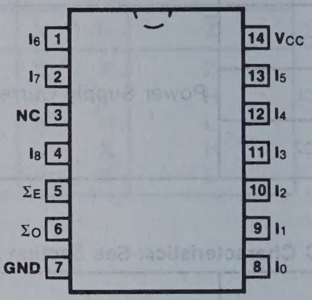
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	2.5	4.0	5.3	2.0	7.5	2.5	6.0	ns	3-1
t_{PHL}		2.0	3.5	4.7	1.5	6.0	2.0	5.5		3-3
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	4.0	6.5	8.5	4.0	12	4.0	9.5	ns	3-1
t_{PHL}		4.0	7.3	9.5	4.0	11.5	4.0	11		3-10
t_{PZH}	Output Enable Time	3.0	5.9	7.5	3.0	11	3.0	8.5	ns	3-1 3-12 3-13
t_{PZL}		3.0	5.5	7.5	3.0	9.5	3.0	8.5		
t_{PHZ}	Output Disable Time	2.0	4.3	6.0	1.5	7.0	2.0	7.0		
t_{PLZ}		2.0	4.5	6.0	2.0	9.0	2.0	7.0		

54F/74F280

9-Bit Parity Generator/Checker

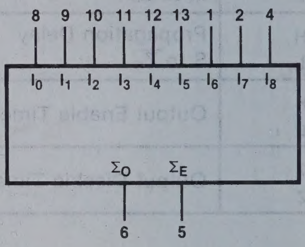
Connection Diagam



Description

The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = −55° C to +125° C	
Plastic DIP (P)	74F280PC		9A
Ceramic DIP (D)	74F280DC	54F280DM	6A
Flatpak (F)		54F280FM	3I

Input Loading/Fan-Out: See Section 3 for U.L. definitions

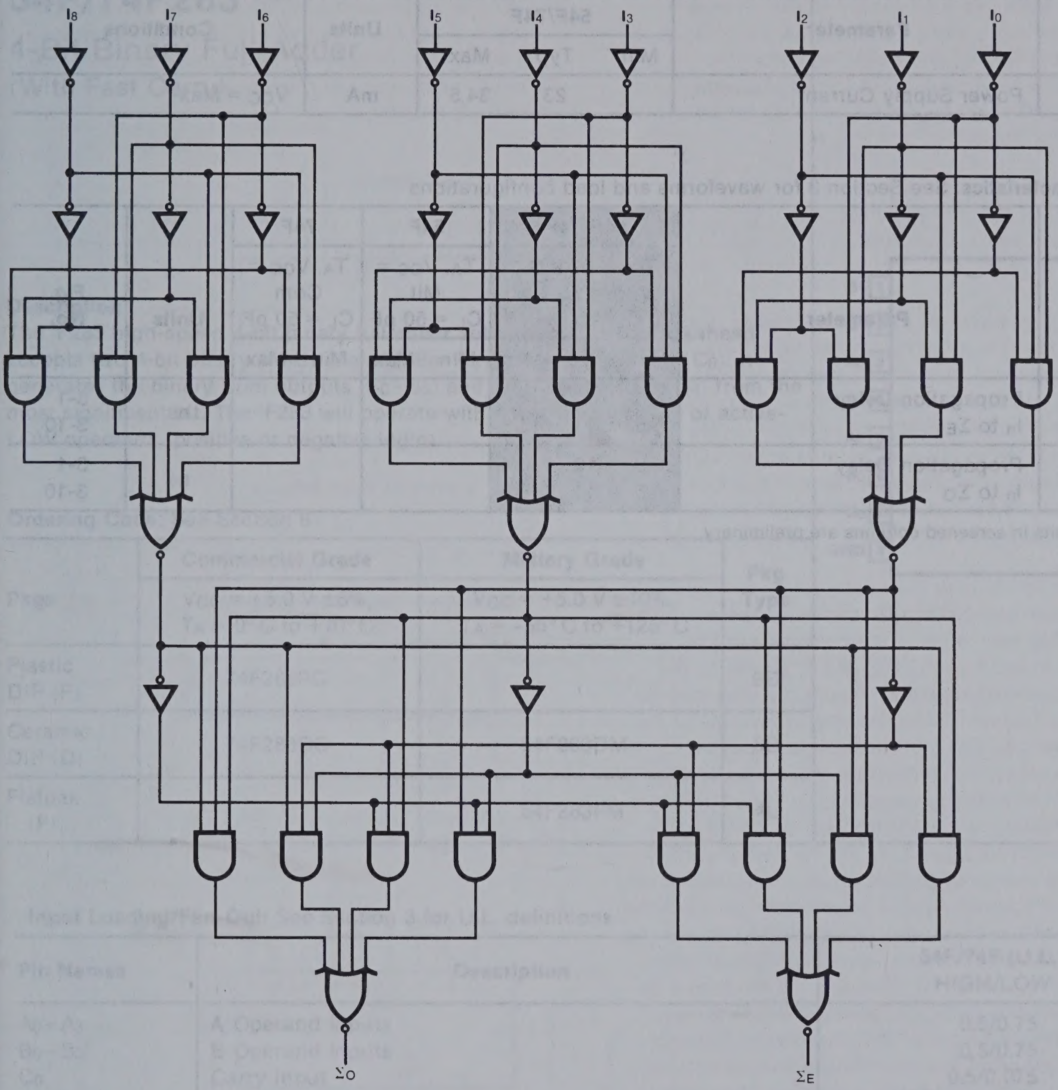
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$I_0 - I_8$	Data Inputs	0.5/0.375
Σ_O	Odd Parity Output	25/12.5
Σ_E	Even Parity Output	25/12.5

Truth Table

NUMBER OF INPUTS $I_0 - I_8$ THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram


I8
I7
I6
I5
I4
I3
I2
I1
I0
ΣO
ΣE

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		23	34.5	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E	6.0 6.5	10 11	14 15.5					ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O	6.0 6.5	10 11	14 15.5					ns	3-1 3-10

▨ Test limits in screened columns are preliminary.

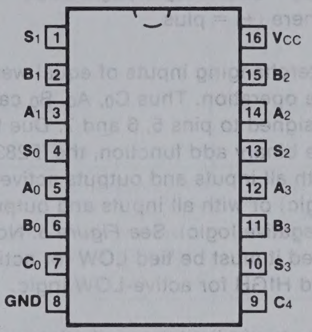
54F/74F283

4-Bit Binary Full Adder
(With Fast Carry)

Description

The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

Connection Diagram



S1 1
B1 2
A1 3
S0 4
A0 5
B0 6
C0 7
GND 8
16 VCC
15 B2
14 A2
13 S2
12 A3
11 B3
10 S3
9 C4

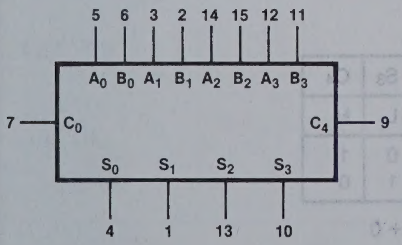
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F283PC		9B
Ceramic DIP (D)	74F283DC	54F283DM	6B
Flatpak (F)		54F283FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	A Operand Inputs	0.5/0.75
$B_0 - B_3$	B Operand Inputs	0.5/0.75
C_0	Carry Input	0.5/0.375
$S_0 - S_3$	Sum Outputs	25/12.5
C_4	Carry Output	25/12.5

Logic Symbol



5
6
3
2
14
15
12
11
A0
B0
A1
B1
A2
B2
A3
B3
7
C0
C4
9
S0
S1
S2
S3
4
1
13
10

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum ($S_0 - S_3$) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See *Figure a*. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure b* shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure c* shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure d* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. *Figure e* shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.

Fig. b 3-Bit Adder

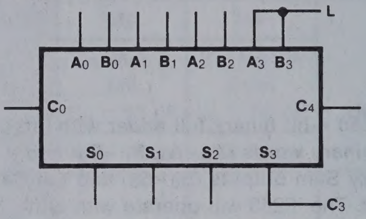


Fig. c 2-Bit and 1-Bit Adders

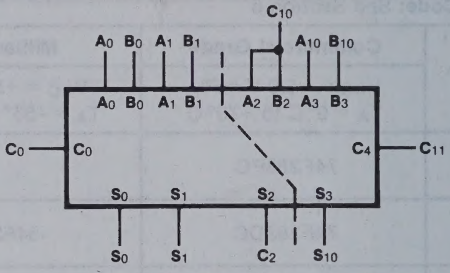


Fig. d 5-Input Encoder

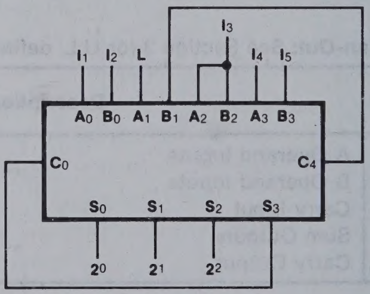
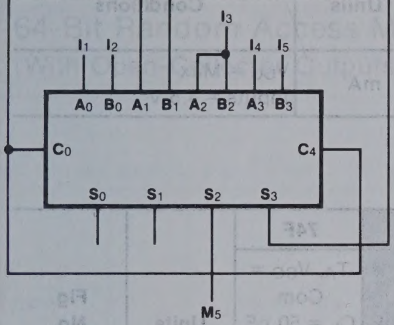


Fig. a Active-HIGH versus Active-LOW Interpretation

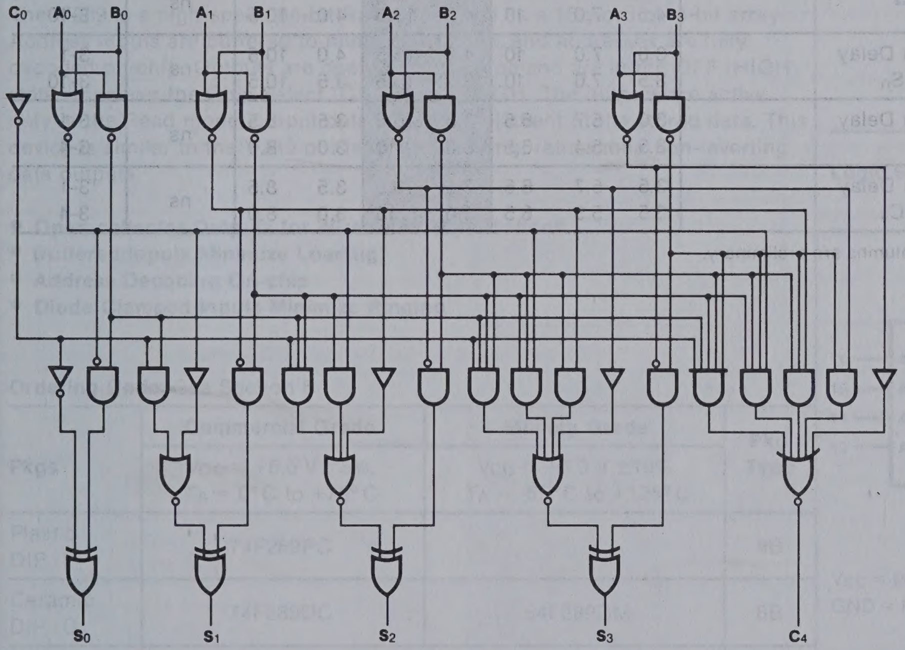
	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

Fig. e 5-Input Majority Gate


I1
I2
I3
I4
I5
A0
B0
A1
B1
A2
B2
A3
B3
C0
C4
S0
S1
S2
S3
M5

Logic Diagram


C0
A0
B0
A1
B1
A2
B2
A3
B3
S0
S1
S2
S3
C4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		36	55	mA	V_{CC} = Max Inputs = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	4.0	7.0	10	3.5	13.5	3.5	10.5	ns	3-1
t_{PHL}	C_0 to S_n	4.5	7.0	10	4.0	13.5	4.0	10.5		3-10
t_{PLH}	Propagation Delay	3.0	7.0	10	4.0	13.5	4.0	10.5	ns	3-1
t_{PHL}	A_n or B_n to S_n	3.5	7.0	10	3.5	13.5	3.5	10.5		3-10
t_{PLH}	Propagation Delay	3.0	5.7	6.5	3.5	10.5	3.5	8.5	ns	3-1
t_{PHL}	C_0 to C_4	3.5	5.4	6.5	3.0	10	3.0	8.0		3-4
t_{PLH}	Propagation Delay	3.5	5.7	6.5	3.5	10.5	3.5	8.5	ns	3-1
t_{PHL}	A_n or B_n to C_4	3.5	5.3	6.5	3.0	10	3.0	8.0		3-4

▨ Test limits in screened columns are preliminary.

54F/74F289

64-Bit Random Access Memory

(With Open-Collector Outputs)

Description

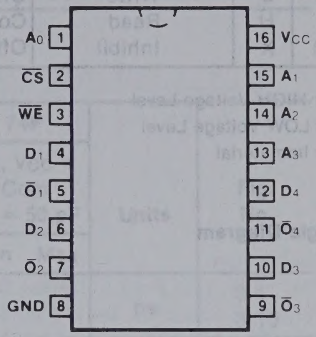
The 'F289 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the OFF (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data. This device is similar to the 'F319 but features inverting, rather than non-inverting, data outputs.

- **Open-collector Outputs for Wired-AND Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-chip**
- **Diode Clamped Inputs Minimize Ringing**

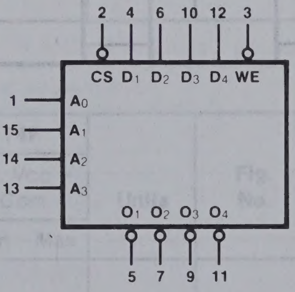
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F289PC		9B
Ceramic DIP (D)	74F289DC	54F289DM	6B
Flatpak (F)		54F289FM	4L

Connection Diagram



Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.75
$D_1 - D_4$	Data Inputs	0.5/0.375
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/12.5

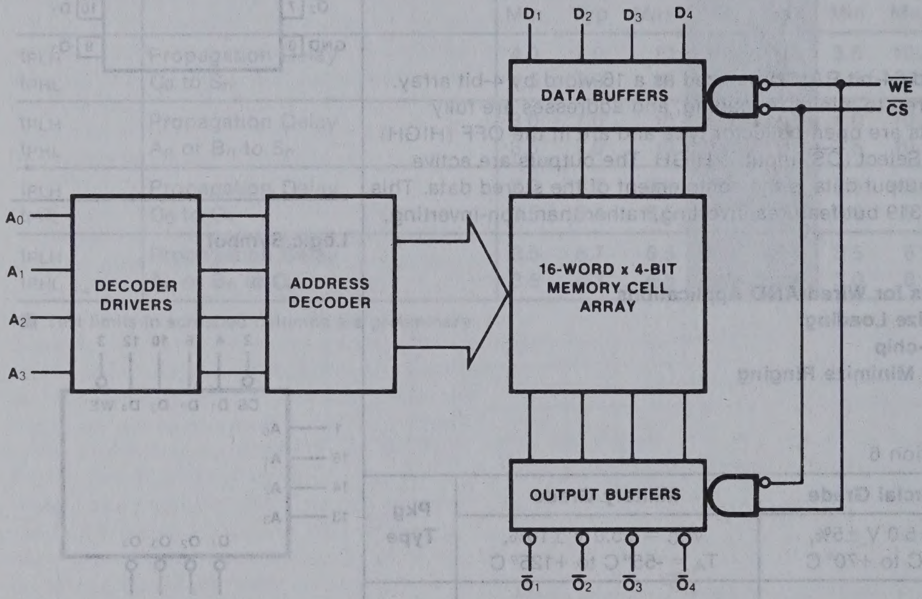
*OC - Open Collector

Function Table

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


D1
D2
D3
D4
DATA BUFFERS
WE
CS
A0
A1
A2
A3
DECODER DRIVERS
ADDRESS DECODER
16-WORD x 4-BIT MEMORY CELL ARRAY
OUTPUT BUFFERS
Ō1
Ō2
Ō3
Ō4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$ = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to $\overline{O}_n$	11 8.0	18 14	25 20					ns	3-1 3-10
t_{PHL}	Access Time $\overline{CS}$ to $\overline{O}_n$	4.5	8.0	11					ns	3-1 3-4
t_{PLH}	Disable Time $\overline{CS}$ to O_n	6.0	10.2	14						
t_{PHL}	Write Recovery Time $\overline{WE}$ to $\overline{O}_n$	8.0	13.5	19					ns	3-1 3-3
t_{PLH}	Disable Time $\overline{WE}$ to $\overline{O}_n$	8.0	13.5	19						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0							ns	3-16
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	10 10							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0								
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	6.0							ns	3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0								
t_w (L)	$\overline{WE}$ Pulse Width LOW	6.0							ns	3-16

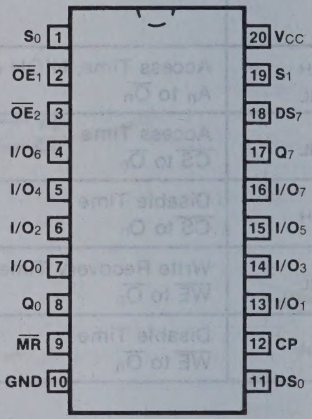
▨ Test limits in screened columns are preliminary.

54F/74F299

8-Input Universal Shift/Storage Register

(With Common Parallel I/O Pins)

Connection Diagram



Description

The 'F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F299PC		9Z
Ceramic DIP (D)	74F299DC	54F299DM	4E
Flatpak (F)		54F299FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
DS_0	Serial Data Input for Right Shift	0.5/0.375
DS_7	Serial Data Input for Left Shift	0.5/0.375
S_0, S_1	Mode Select Inputs	0.5/0.75
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.375
$I/O_0 - I/O_7$	Parallel Data Inputs or 3-State Parallel Outputs	0.5/0.375 25/12.5
Q_0, Q_7	Serial Outputs	25/12.5

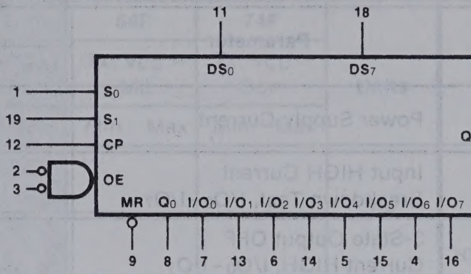
Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE_1}$ or $\overline{OE_2}$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Logic Symbol



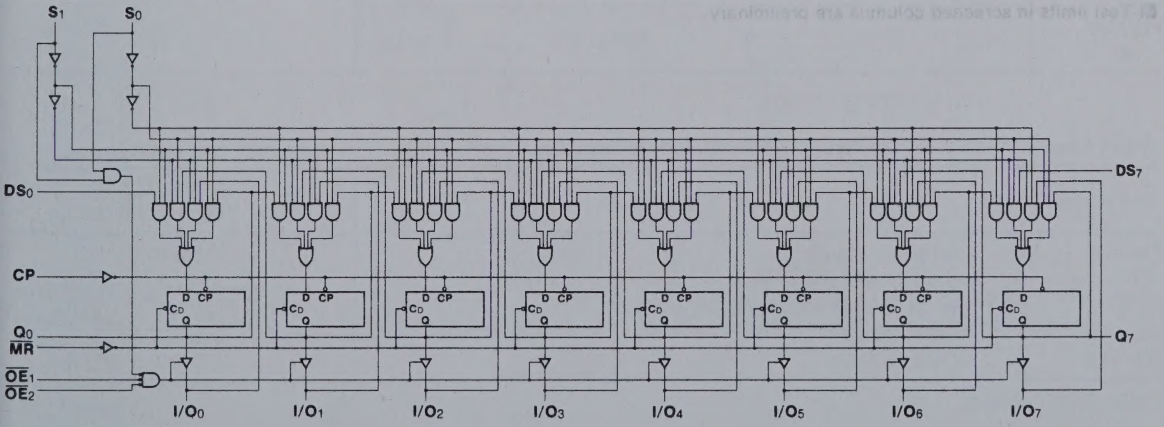
V_{CC} = Pin 20
GND = Pin 10

Mode Select Table

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		68	95	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V CP = HIGH
I_{IH}	Input HIGH Current Breakdown Test, $I/O_0 - I/O_7$			100	µA	V_{CC} = Max, V_{IN} = 5.5 V
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, $I/O_0 - I/O_7$			70	µA	V_{CC} = Max, V_{OUT} = 2.4 V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, $I/O_0 - I/O_7$			-650	µA	V_{CC} = Max, V_{OUT} = 0.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	70							MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.5 5.5	10 10	14 14					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	5.5 5.5	10 10	14 14						
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	6.5	12	16					ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	6.5	12	16						
t_{PZH} t_{PZL}	Output Enable Time	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	4.0 4.0	7.0 7.0	10 10						

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW S_0 or S_1 to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	0 0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	7.0 7.0							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	7.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0							ns	3-11

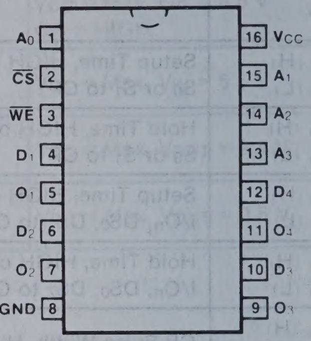
▨ Test limits in screened columns are preliminary.

54F/74F319

64-Bit Random Access Memory

(With Open-Collector Outputs)

Connection Diagram

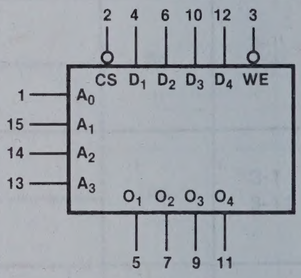


Description

The 'F319 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the OFF (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F289 but features non-inverting, rather than inverting, data outputs.

- **Open-collector Outputs for Wired-AND Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-chip**
- **Diode Clamped Inputs Minimize Ringing**

Logic Symbol



VCC = Pin 16
GND = Pin 8

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F319PC		9B
Ceramic DIP (D)	74F319DC	54F319DM	6B
Flatpak (F)		54F319FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.75
$D_1 - D_4$	Data Inputs	0.5/0.375
$O_1 - O_4$	Data Outputs	OC*/12.5

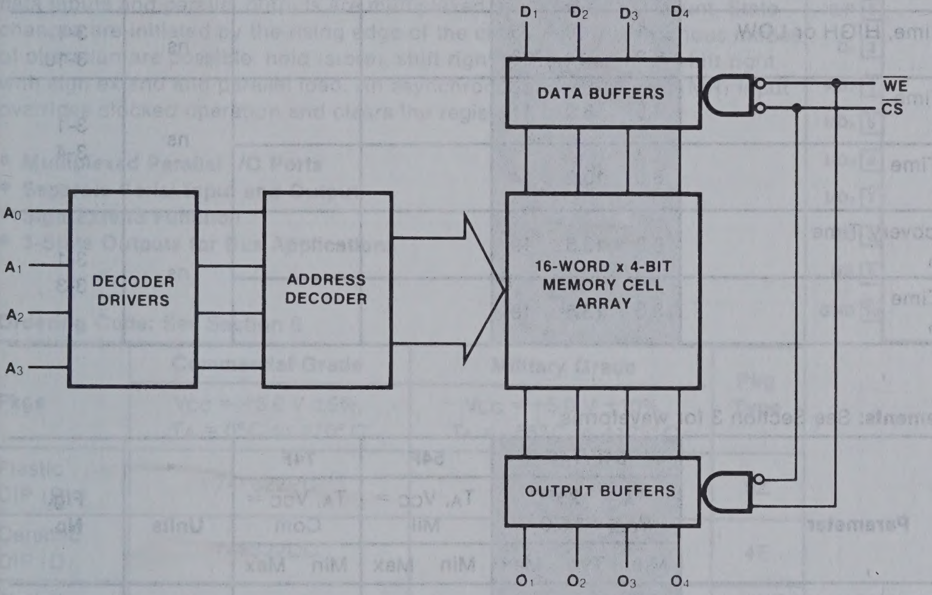
*OC - Open Collector

Function Table

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


D₁
D₂
D₃
D₄
DATA BUFFERS
$\overline{WE}$
$\overline{CS}$
A₀
A₁
A₂
A₃
DECODER DRIVERS
ADDRESS DECODER
16-WORD x 4-BIT MEMORY CELL ARRAY
OUTPUT BUFFERS
O₁
O₂
O₃
O₄

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$ = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to O_n	11 8.0	18 14	25 20					ns	3-1 3-10
t_{PHL}	Access Time $\overline{CS}$ to O_n	4.5	8.0	11					ns	3-1 3-4
t_{PLH}	Disable Time $\overline{CS}$ to O_n	6.0	10.2	14						
t_{PHL}	Write Recovery Time $\overline{WE}$ to O_n	8.0	13.5	19					ns	3-1 3-3
t_{PLH}	Disable Time $\overline{WE}$ to O_n	8.0	13.5	19						

AC Operating Requirements: See Section 3 for waveforms

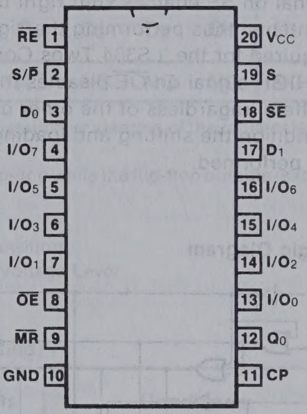
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0							ns	3-16
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	10 10							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0								
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	6.0							ns	3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0								
t_w (L)	$\overline{WE}$ Pulse Width LOW	6.0							ns	3-16

▨ Test limits in screened columns are preliminary.

54F/74F322

8-Bit Serial/Parallel Register
(With Sign Extend)

Connection Diagram



Description

The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

- **Multiplexed Parallel I/O Ports**
- **Separate Serial Input and Output**
- **Sign Extend Function**
- **3-State Outputs for Bus Applications**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = −55° C to +125° C	
Plastic DIP (P)	74F322PC		9Z
Ceramic DIP (D)	74F322DC	54F322DM	4E
Flatpak (F)		54F322FM	4D

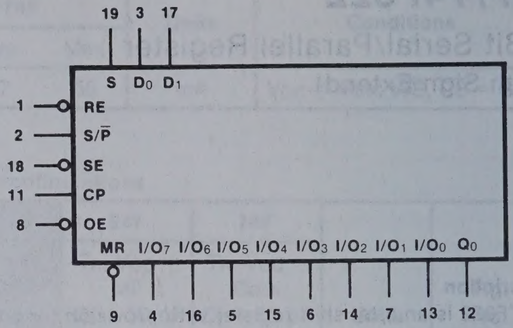
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{RE}$	Register Enable Input (Active LOW)	0.5/0.375
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	0.5/0.375
$\overline{SE}$	Sign Extend Input (Active LOW)	0.5/1.125
S	Serial Data Select Input	0.5/0.75
D_0, D_1	Serial Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
Q_0	Bi-state Serial Output	25/12.5
I/O_0 - I/O_7	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs	0.5/0.375 25/12.5

Functional Description

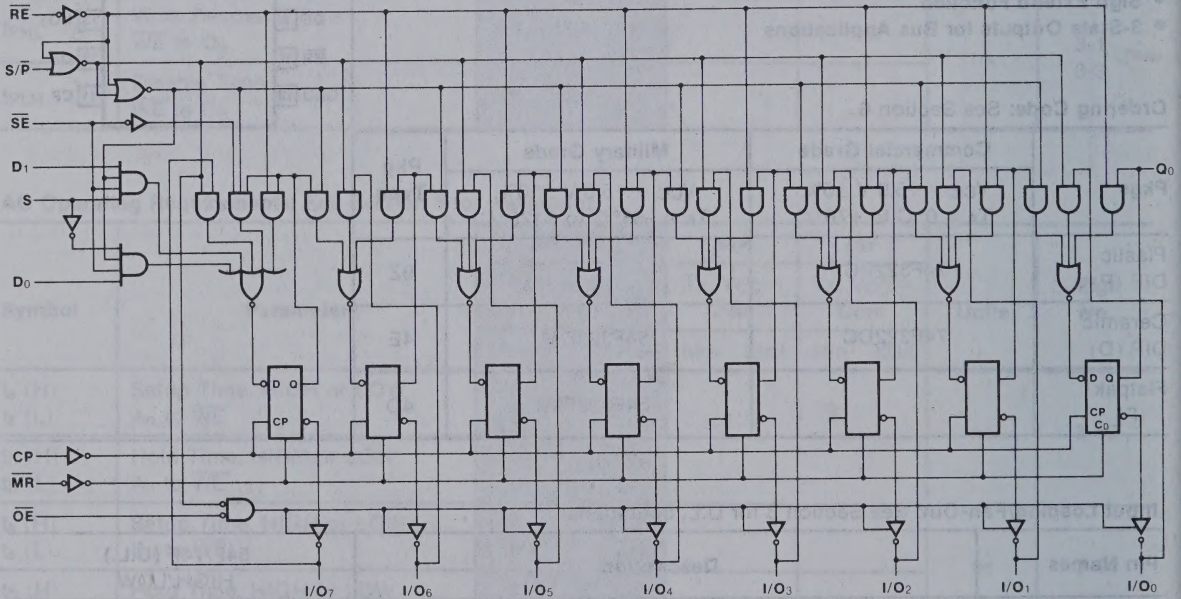
The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the 'LS384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Logic Symbol


19
3
17
S
D0
D1
1
RE
2
S/P
18
SE
11
CP
8
OE
MR
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
I/O0
Q0
9
4
16
5
15
6
14
7
13
12

V_{CC} = Pin 20
GND = Pin 10

Logic Diagram


RE
S/P
SE
D1
S
D0
CP
MR
OE
D Q
CP
CD
Q0
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
I/O0

Mode Select Table

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L L	X X	X X	X X	X X	L H	X X	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L L
Parallel Load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H H	L L	H H	H H	L H	L L	↑ ↑	D_0 D_1	O_7 O_7	O_6 O_6	O_5 O_5	O_4 O_4	O_3 O_3	O_2 O_2	O_1 O_1	O_1 O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected

1. $I_7 - I_0$ = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. $O_7 - O_0$ = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		60	84	mA	V_{CC} = Max, CP = HIGH Output Disabled
I_{IH}	Input HIGH Current Breakdown Test, $I/O_0 - I/O_7$			100	μA	V_{CC} = Max, V_{IN} = 5.5 V
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, $I/O_0 - I/O_7$			70	μA	V_{CC} = Max, V_{OUT} = 2.4 V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, $I/O_0 - I/O_7$			-650	μA	V_{CC} = Max, V_{OUT} = 0.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70							MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	5.5 5.5	10 10	14 14					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0	5.5 5.5	10 10	14 14						
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	6.5	12	16					ns	3-1 3-11

▨ Test limits in screened columns are preliminary.

AC Characteristics (cont'd): See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0	6.5	12	16					ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	4.0 4.0	7.0 7.0	10 10						
t_{PZH} t_{PZL}	Output Enable Time $S/\overline{P}$ to I/O_n	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $S/\overline{P}$ to I/O_n	4.0 4.0	7.0 7.0	10 10						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{RE}$ to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{RE}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_0, D_1 or I/O_n to CP	5.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_0, D_1 or I/O_n to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{SE}$ to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{SE}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $S/\overline{P}$ to CP	12 12							ns	3-5
t_s (H) t_s (L)	Setup Time, HIGH or LOW S to CP	12 12								
t_h (H) t_h (L)	Hold Time, HIGH or LOW S or $S/\overline{P}$ to CP	0 0								
t_w (H)	CP Pulse Width HIGH	7.0							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	7.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0							ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F323

8-Bit Universal Shift/Storage Register

(With Synchronous Reset and Common I/O Pins)

Description

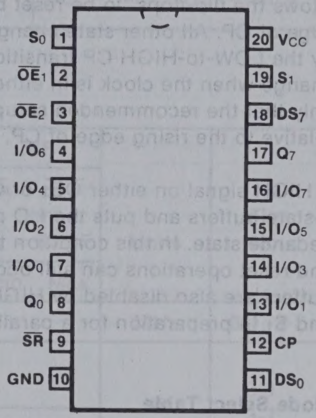
The 'F323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F323PC		9Z
Ceramic DIP (D)	74F323DC	54F323DM	4E
Flatpak (F)		54F323FM	4D

Connection Diagram



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
DS_0	Serial Data Input for Right Shift	0.5/0.375
DS_7	Serial Data Input for Left Shift	0.5/0.375
S_0, S_1	Mode Select Inputs	0.5/0.75
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.375
$I/O_0 - I/O_7$	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs	0.5/0.75 25/12.5
Q_0, Q_7	Serial Outputs	25/12.5

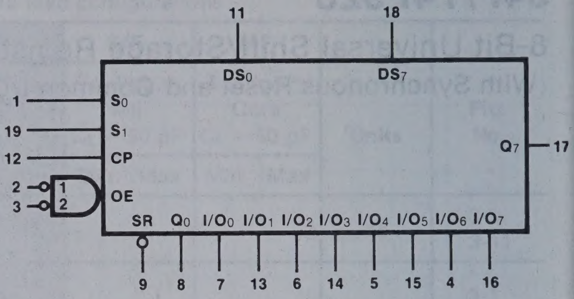
Functional Description

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Logic Symbol



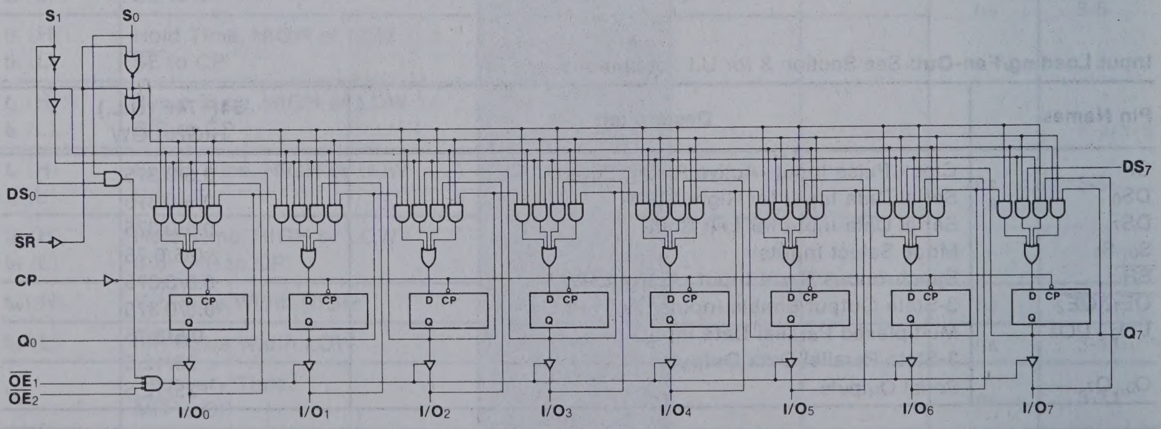
VCC = Pin 20
GND = Pin 10

Mode Select Table

INPUTS				RESPONSE
$\overline{SR}$	S_1	S_0	CP	
L	X	X		Synchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H		Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H		Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L		Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		66	92	mA	V_{CC} = Max, CP = HIGH Outputs Disabled
I_{IH}	Input HIGH Current Breakdown Test, $I/O_0 - I/O_7$			100	μA	V_{CC} = Max, V_{IN} = 5.5 V
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, $I/O_0 - I/O_7$			70	μA	V_{CC} = Max, V_{OUT} = 2.4 V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, $I/O_0 - I/O_7$			−650	μA	V_{CC} = Max, V_{OUT} = 0.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	70							MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.5 5.5	10 10	14 14					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	5.5 5.5	10 10	14 14						
t_{PZH} t_{PZL}	Output Enable Time	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	4.0 4.0	7.0 7.0	10 10						

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW S_0 or S_1 to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{SR}$ to CP	15 15							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0 0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	7.0 7.0							ns	3-7

▨ Test limits in screened columns are preliminary.

54F/74F350

4-Bit Shifter

(With 3-State Outputs)

Description

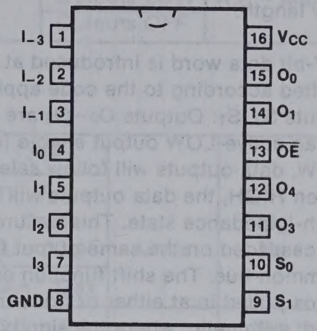
The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

- **Linking Inputs for Word Expansion**
- **3-State Outputs for Extending Shift Range**

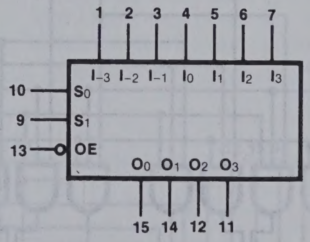
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F350PC		9B
Ceramic DIP (D)	74F350DC	54F350DM	6B
Flatpak (F)		54F350FM	4L

Connection Diagram



Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S_0, S_1	Select Inputs	0.5/0.75
I_{-3} – I_3	Data Inputs	0.5/0.75
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
O_0 – O_3	3-State Outputs	25/12.5

Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1. Outputs $O_0 - O_3$ are 3-state, controlled by an active-LOW output enable ($\overline{OE}$). When $\overline{OE}$ is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

Logic Equations

$$O_0 = \overline{S_0}\,\overline{S_1}\,I_0 + S_0\,\overline{S_1}\,I_{-1} + \overline{S_0}\,S_1\,I_{-2} + S_0\,S_1\,I_{-3}$$

$$O_1 = \overline{S_0}\,\overline{S_1}\,I_1 + S_0\,\overline{S_1}\,I_0 + \overline{S_0}\,S_1\,I_{-1} + S_0\,S_1\,I_{-2}$$

$$O_2 = \overline{S_0}\,\overline{S_1}\,I_2 + S_0\,\overline{S_1}\,I_1 + \overline{S_0}\,S_1\,I_0 + S_0\,S_1\,I_{-1}$$

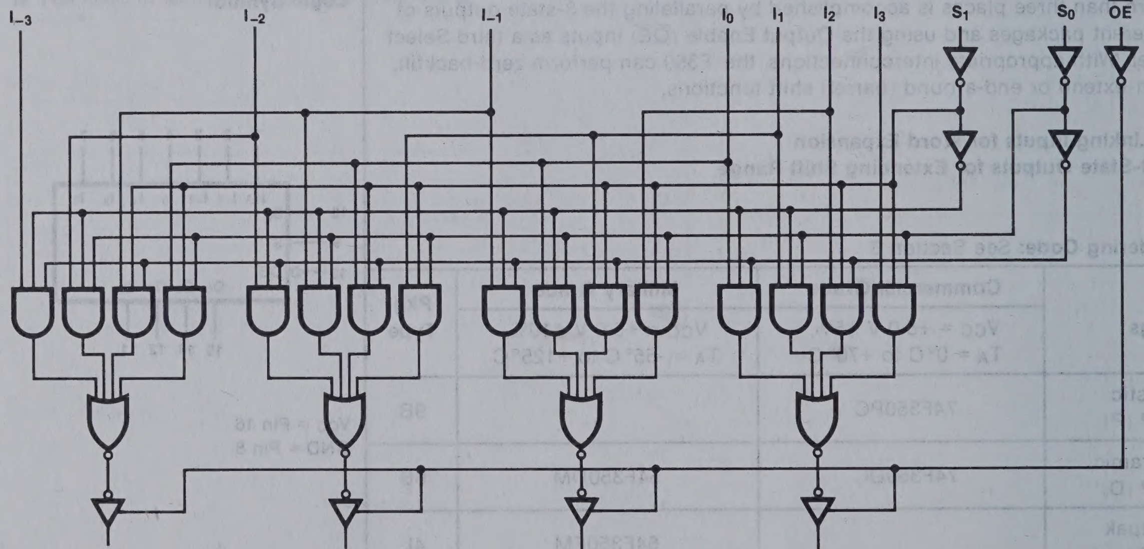
$$O_3 = \overline{S_0}\,\overline{S_1}\,I_3 + S_0\,\overline{S_1}\,I_2 + \overline{S_0}\,S_1\,I_1 + S_0\,S_1\,I_0$$

Truth Table

INPUTS			OUTPUTS			
$\overline{OE}$	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		22	35	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			26	41		Outputs LOW	
I_{CCZ}			26	42		Outputs OFF	

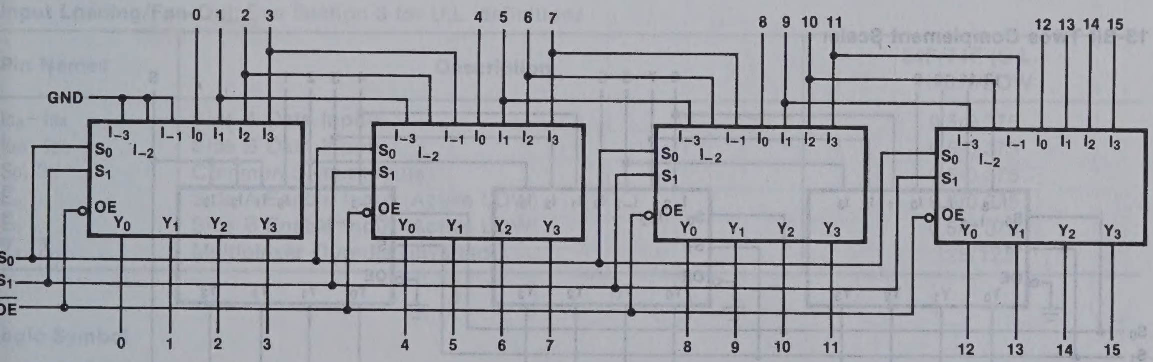
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to O_n	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.5 7.0	3.0 2.5	7.0 6.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay S_n to O_n	4.0 3.0	7.8 6.5	10 8.5	4.0 3.0	13 10	4.0 3.0	11 9.5	ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.5 11	2.5 4.0	8.0 10	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	7.0 8.5	2.0 2.0	6.5 6.5		

▨ Test limits in screened columns are preliminary.

Applications

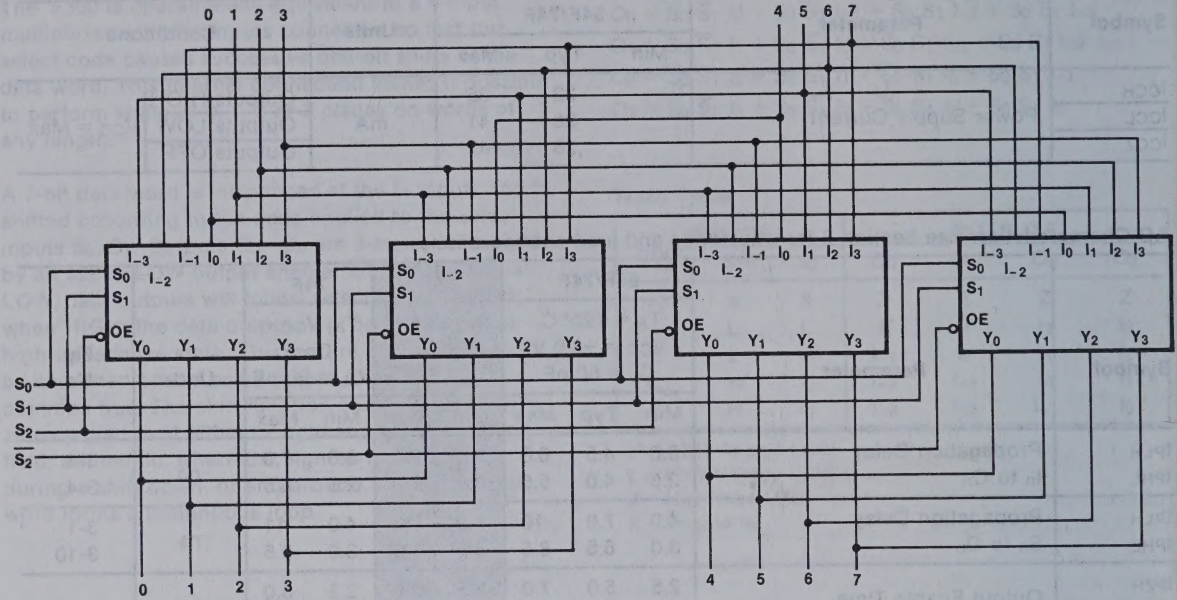
16-Bit Shift-Up 0 to 3 Places, Zero Backfill



0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
GND
I_{-3} I_{-2} I_{-1} I_0 I_1 I_2 I_3
S_0
S_1
OE
Y_0 Y_1 Y_2 Y_3
S_0
S_1
$\overline{OE}$
0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15

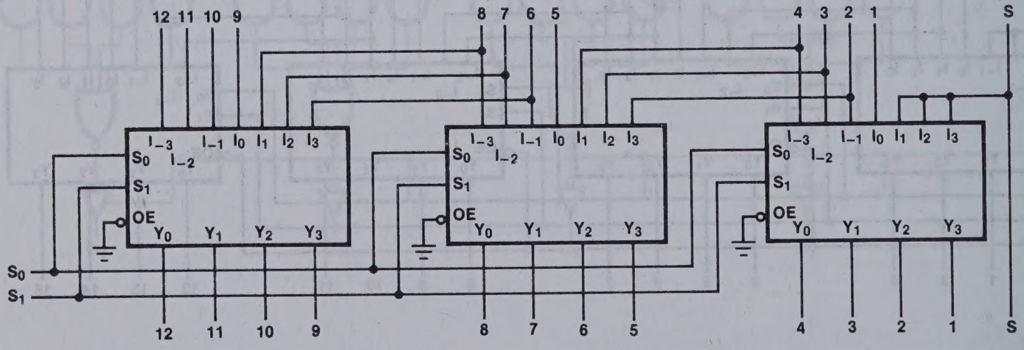
$_1$	S$_0$	
	L	NO SHIFT
	H	SHIFT 1 PLACE
	L	SHIFT 2 PLACES
	H	SHIFT 3 PLACES

8-Bit End Around Shift 0 to 7 Places


0 1 2 3
4 5 6 7
I₋₃ I₋₂ I₋₁ I₀ I₁ I₂ I₃
S₀
S₁
OE
Y₀ Y₁ Y₂ Y₃
S₀
S₁
S₂
S̄₂
0 1 2 3
4 5 6 7

S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-Bit Twos Complement Scaler

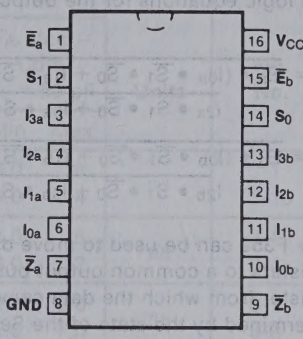

12 11 10 9
8 7 6 5
4 3 2 1
S
I₋₃ I₋₂ I₋₁ I₀ I₁ I₂ I₃
S₀
S₁
OE
Y₀ Y₁ Y₂ Y₃
S₀
S₁
12 11 10 9
8 7 6 5
4 3 2 1
S

S_1	S_0		SCALE
L	L	÷ 8	1/8
L	H	÷ 4	1/4
H	L	÷ 2	1/2
H	H	NO CHANGE	1

54F/74F352

Dual 4-Input Multiplexer

Connection Diagram


$\overline{E}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
$\overline{Z}_a$ 7
GND 8
16 V_{CC}
15 $\overline{E}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

Description

The 'F352 is a very high speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- **Inverted Version of the 'F153**
- **Separate Enables for Each Multiplexer**
- **Input Clamp Diode Limits High Speed Termination Effects**

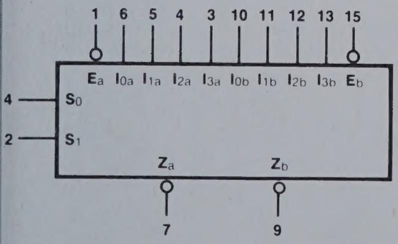
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F352PC		9B
Ceramic DIP (D)	74F352DC	54F352DM	6B
Flatpak (F)		54F352FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
I_{0a} - I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} - I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs (Inverted)	25/12.5

Logic Symbol


1
6
5
4
3
10
11
12
13
15
E_a
I_{0a}
I_{1a}
I_{2a}
I_{3a}
I_{0b}
I_{1b}
I_{2b}
I_{3b}
E_b
4
S_0
2
S_1
Z_a
Z_b
7
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{E_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

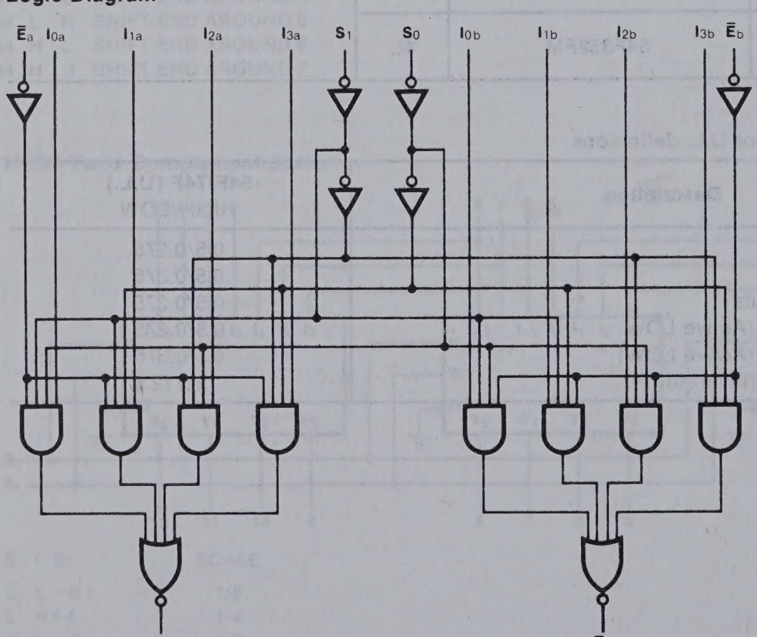
The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

Truth Table

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current		9.3 13.3	14 20	mA	V_{IN} = Gnd V_{IN} = HIGH	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	4.0 4.0	7.4 7.0	13 13	3.5 3.5	14.5 15	4.0 4.0	14 14	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0 4.0	8.7 8.6	14 11	4.5 4.0	17 13	5.0 4.0	15 12	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.0 2.0	4.9 3.0	7.0 6.0	2.0 2.0	9.0 7.5	2.0 2.0	8.0 7.0	ns	3-1 3-3

▨ Test limits in screened columns are preliminary.

54F/74F353

Dual 4-Input Multiplexer

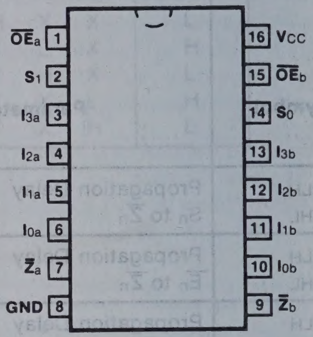
(With 3-State Outputs)

Description

The 'F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- **Inverted Version of 'F253**
- **Multifunction Capability**
- **Separate Enables for Each Multiplexer**

Connection Diagram



$\overline{OE}_a$ 1
S_1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
$\overline{Z}_a$ 7
GND 8
16 V_{CC}
15 $\overline{OE}_b$
14 S_0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

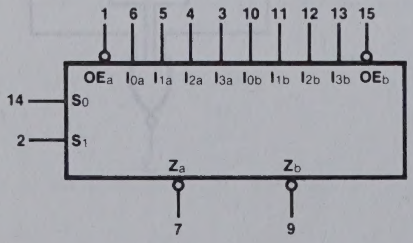
Ordering Code: See Section 6

Pkg	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F353PC		9B
Ceramic DIP (D)	74F353DC	54F353DM	6B
Flatpak (F)		54F353FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
I_{0a} - I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} - I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs (Inverted)	25/12.5

Logic Symbol



1
6
5
4
3
10
11
12
13
15
OE_a
I_{0a}
I_{1a}
I_{2a}
I_{3a}
I_{0b}
I_{1b}
I_{2b}
I_{3b}
OE_b
14
S_0
2
S_1
Z_a
Z_b
7
9

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

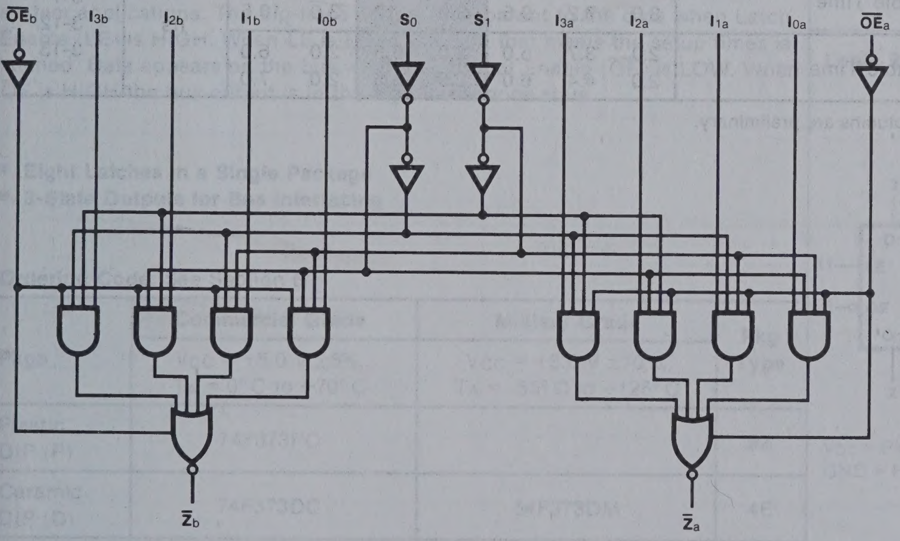
Truth Table

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Logic Diagram



4

DC Characteristics Over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
I_{CCH}	Power Supply Current		9.3	14	mA	I_n, S_n, $\overline{OE}_n$ = Gnd	V_{CC} = Max
I_{CCL}			13.3	20		I_n, S_n = Gnd	
I_{CCZ}			15	23		$\overline{OE}_n$ = 4.5 V	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			54F ▨ T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0 4.0	8.8 7.4	14 11	5.0 4.0	16 14	5.0 4.0	15 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.0 2.0	5.6 2.8	7.0 6.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.0	ns	3-1 3-3
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.8 7.2	9.0 9.5	3.0 3.0	11 12	3.0 3.0	10 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.5	2.0 2.0	6.0 7.0		

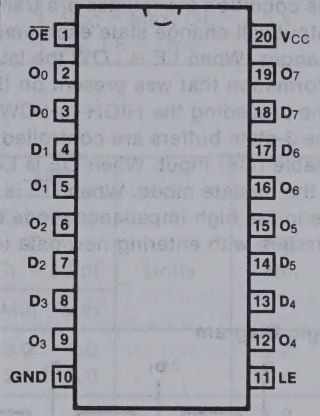
▨ Test limits in screened columns are preliminary.

54F/74F373

Octal Transparent Latch

(With 3-State Outputs)

Connection Diagram

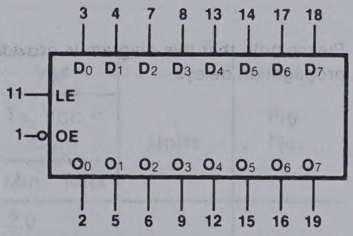

$\overline{OE}$ 1
O_0 2
D_0 3
D_1 4
O_1 5
O_2 6
D_2 7
D_3 8
O_3 9
GND 10
20 V_{CC}
19 O_7
18 D_7
17 D_6
16 O_6
15 O_5
14 D_5
13 D_4
12 O_4
11 LE

Description

The 'F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

Logic Symbol


3
4
7
8
13
14
17
18
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
11
LE
1
OE
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
2
5
6
9
12
15
16
19

V_{CC} = Pin 20
GND = Pin 10

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0\ V \pm 10\%$, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F373PC		9Z
Ceramic DIP (D)	74F373DC	54F373DM	4E
Flatpak (F)		54F373FM	4D

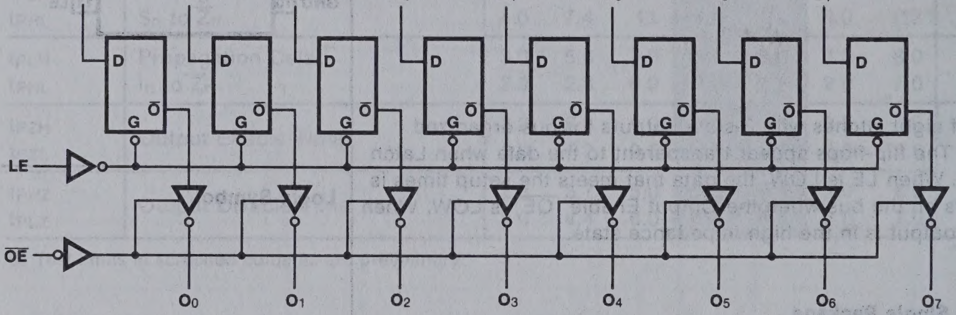
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$O_0 - O_7$	3-State Latch Outputs	25/12.5

Functional Description

The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		35	55	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns	3-2
t_{PHL}	D_n to O_n	2.0	3.7	5.0	2.0	6.0	2.0	6.0		3-4
t_{PLH}	Propagation Delay	5.0	9.0	11.5	5.0	15	5.0	13	ns	3-2
t_{PHL}	LE to O_n	3.0	5.2	7.0	3.0	8.5	3.0	8.0		3-7
t_{PZH}	Output Enable Time	2.0	5.0	11	2.0	13.5	2.0	12	ns	3-2
t_{PZL}		2.0	5.6	7.5	2.0	10	2.0	8.5		3-12 3-13
t_{PHZ}	Output Disable Time	2.0	4.5	6.5	2.0	10	2.0	7.5	ns	3-2
t_{PLZ}		2.0	3.8	5.0	2.0	7.0	2.0	6.0		3-12 3-13

AC Operating Requirements: See Section 6 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	2.0			2.0		2.0		ns	3-15
t_s (L)	D_n to LE	2.0			2.0		2.0			
t_h (H)	Hold Time, HIGH or LOW	3.0			3.0		3.0			
t_h (L)	D_n to LE	3.0			3.0		3.0			
t_w (H)	LE Pulse Width HIGH	6.0			6.0		6.0		ns	3-7

54F/74F374

Octal D-Type Flip-Flop
(With 3-State Outputs)

Description

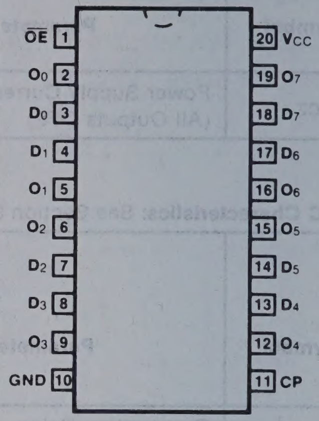
The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 6

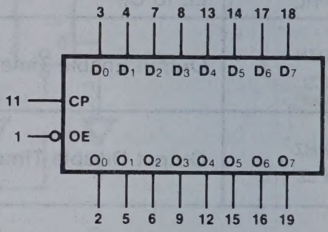
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F374PC		9Z
Ceramic DIP (D)	74F374DC	54F374DM	4E
Flatpak (F)		54F374FM	4D

Connection Diagram



$\overline{OE}$ 1
O_0 2
D_0 3
D_1 4
O_1 5
O_2 6
D_2 7
D_3 8
O_3 9
GND 10
20 V_{CC}
19 O_7
18 D_7
17 D_6
16 O_6
15 O_5
14 D_5
13 D_4
12 O_4
11 CP

Logic Symbol



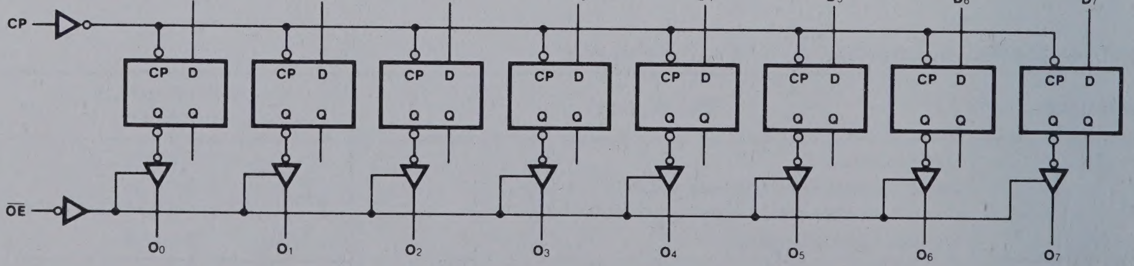
3 4 7 8 13 14 17 18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 OE
O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$O_0 - O_7$	3-State Outputs	25/12.5

Logic Diagram



D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
CP
CP D
Q Q
$\overline{OE}$
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7

Functional Description

The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

INPUTS		OUTPUTS	
D_n	CP	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CCL}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100			60		70		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10	ns	3-1
t_{PHL}	CP to O_n	4.0	6.5	8.5	4.0	11	4.0	10		3-7
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14	2.0	12.5	ns	3-1
t_{PZL}		2.0	5.8	7.5	2.0	10	2.0	8.5		3-12
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0		3-13
t_{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	2.0			2.5		2.0		ns	3-5
t_s (L)	D_n to CP	2.0			2.0		2.0			
t_h (H)	Hold Time, HIGH or LOW	2.0			2.0		2.0			
t_h (L)	D_n to CP	2.0			2.5		2.0			
t_w (H)	CP Pulse Width, HIGH or LOW	7.0			7.0		7.0		ns	3-7
t_w (L)		6.0			6.0		6.0			

54F/74F378

Parallel D Register
(With Enable)

Description
The 'F378 is a 6-bit register with a buffered common enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

- **6-Bit High-speed Parallel Register**
- **Positive Edge-Triggered D-Type Inputs**
- **Fully Buffered Common Clock and Enable Inputs**
- **Input Clamp Diodes Limit High Speed Termination Effects**
- **Full TTL and CMOS Compatible**

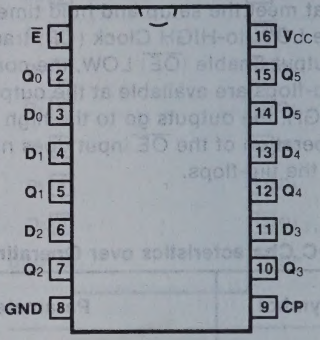
Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F378PC		9B
Ceramic DIP (D)	74F378DC	54F378DM	6B
Flatpak (F)		54F378FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

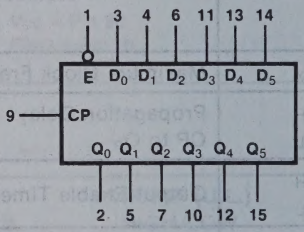
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
$D_0 - D_5$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$Q_0 - Q_5$	Outputs	25/12.5

Connection Diagram



Ē 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 VCC
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

Logic Symbol



1
3
4
6
11
13
14
E
D0
D1
D2
D3
D4
D5
9
CP
Q0
Q1
Q2
Q3
Q4
Q5
2
5
7
10
12
15

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

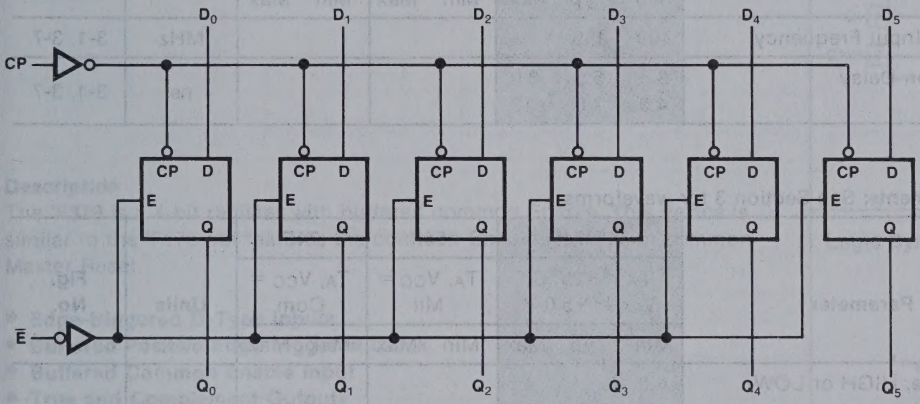
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	_/‾	X	No change
L	_/‾	H	H
L	_/‾	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	100	140						MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 4.5	5.5 7.0	8.0 10					ns	3-1, 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	4.0 4.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	1.0 1.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{E}$ to CP	6.0 6.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{E}$ to CP	0 0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.0 5.0							ns	3-7

▨ Test limits in screened columns are preliminary.

54F/74F379

Quad Parallel Register

(With Enable)

Description

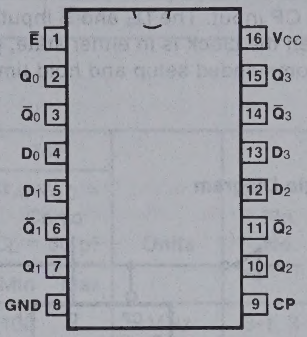
The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **Buffered Common Enable Input**
- **True and Complement Outputs**

Ordering Code: See Section 6

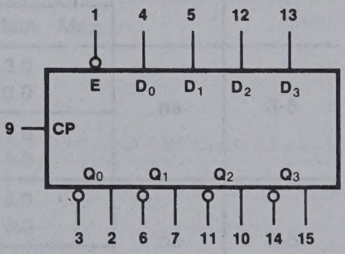
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F379PC		9B
Ceramic DIP (D)	74F379DC	54F379DM	6B
Flatpak (F)		54F379FM	4L

Connection Diagram



$\overline{E}$ 1
Q_0 2
$\overline{Q}_0$ 3
D_0 4
D_1 5
$\overline{Q}_1$ 6
Q_1 7
GND 8
16 V_{CC}
15 Q_3
14 $\overline{Q}_3$
13 D_3
12 D_2
11 $\overline{Q}_2$
10 Q_2
9 CP

Logic Symbol



1
4
5
12
13
E
D_0
D_1
D_2
D_3
9
CP
Q_0
Q_1
Q_2
Q_3
3
2
6
7
11
10
14
15

V_{CC} = Pin 16
GND = Pin 8

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
$D_0 - D_3$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	25/12.5

Functional Description

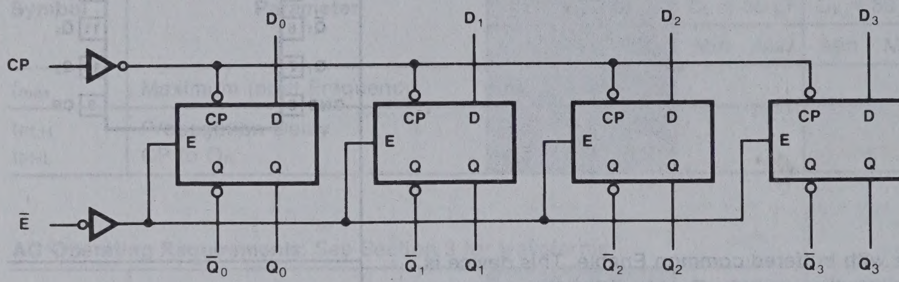
The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
NC = No Change

Logic Diagram



D_0
D_1
D_2
D_3
CP
$\overline{E}$
CP
D
E
Q
Q
$\overline{Q}_0$
Q_0
$\overline{Q}_1$
Q_1
$\overline{Q}_2$
Q_2
$\overline{Q}_3$
Q_3

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		28	40	mA	V_{CC} = Max; D, $\overline{E}$ = Gnd CP = _|¯

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140				100		MHz	3-1, 3-7
t_{PLH}	Propagation Delay	4.0	5.0	6.5			4.0	7.5	ns	3-1
t_{PHL}	CP to Q_n, $\overline{Q}_n$	5.0	6.5	8.5			5.0	9.5		3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	3.0					3.0		ns	3-5
t_s (L)	D_n to CP	3.0					3.0			
t_h (H)	Hold Time, HIGH or LOW	1.0					1.0			
t_h (L)	D_n to CP	1.0					1.0			
t_s (H)	Setup Time, HIGH or LOW	6.0					6.0		ns	3-5
t_s (L)	$\overline{E}$ to CP	6.0					6.0			
t_h (H)	Hold Time, HIGH or LOW	0					0			
t_h (L)	$\overline{E}$ to CP	0					0			
t_w (H)	CP Pulse Width, HIGH or LOW	4.0					4.0		ns	3-7
t_w (L)		5.0					5.0			

54F/74F381

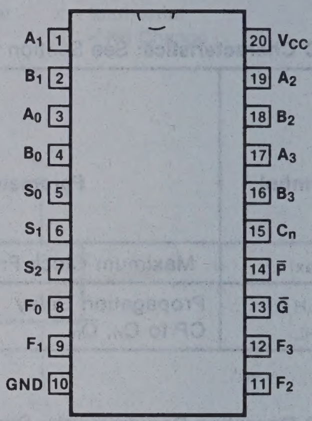
4-Bit Arithmetic Logic Unit

Description

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lenghts. For ripple expansion, refer to the 'F382 ALU data sheet.

- **Low Input Loading Minimizes Drive Requirements**
- **Performs Six Arithmetic and Logic Functions**
- **Selectable Low (Clear) and High (Preset) Functions**
- **Carry Generate and Propagate Outputs for use with Carry Lookahead Generator**

Connection Diagram


A_1 1
B_1 2
A_0 3
B_0 4
S_0 5
S_1 6
S_2 7
F_0 8
F_1 9
GND 10
20 V_{CC}
19 A_2
18 B_2
17 A_3
16 B_3
15 C_n
14 $\overline{P}$
13 $\overline{G}$
12 F_3
11 F_2

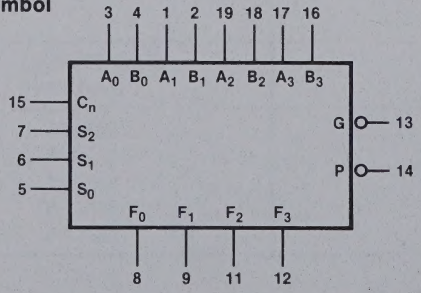
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F381PC		9Z
Ceramic DIP (D)	74F381DC	54F381DM	4E
Flatpak (F)		54F381FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

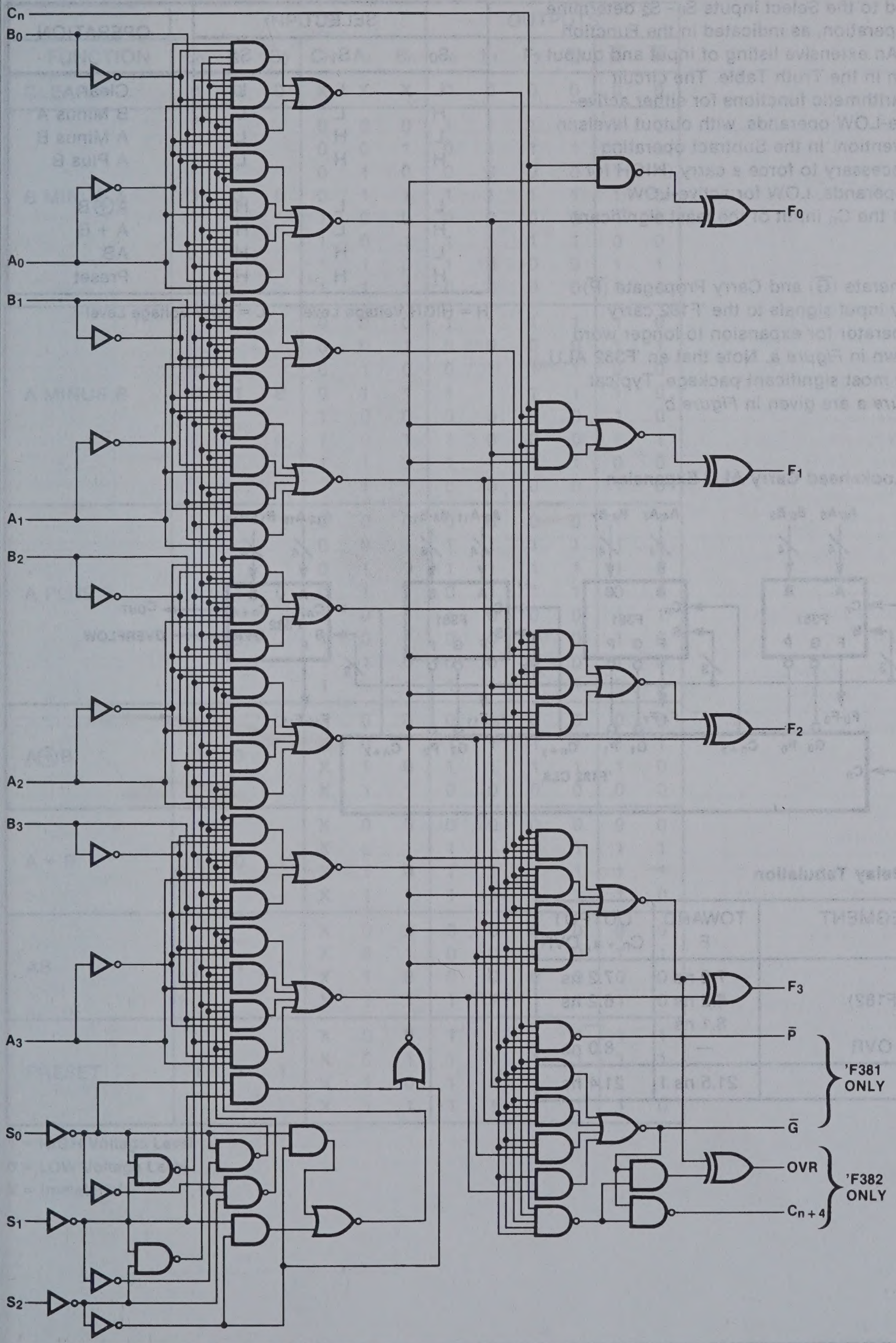
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	A Operand Inputs	0.5/1.50
$B_0 - B_3$	B Operand Inputs	0.5/1.50
$S_0 - S_2$	Function Select Inputs	0.5/0.375
C_n	Carry Input	0.5/1.50
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5
$F_0 - F_3$	Function Outputs	25/12.5

Logic Symbol


3
4
1
2
19
18
17
16
A_0
B_0
A_1
B_1
A_2
B_2
A_3
B_3
15
C_n
7
S_2
6
S_1
5
S_0
G
13
P
14
F_0
F_1
F_2
F_3
8
9
11
12

V_{CC} = Pin 20
GND = Pin 10

Logic Diagram


Cn
B0
A0
B1
A1
B2
A2
B3
A3
S0
S1
S2
F0
F1
F2
F3
P̄
'F381 ONLY
Ḡ
OVR
Cn + 4
'F382 ONLY

Functional Description

Signals applied to the Select inputs $S_0 - S_2$ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH operands, LOW for active-LOW operands) into the C_n input of the least significant package.

Function Select Table

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level   L = LOW Voltage Level

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in *Figure a*. Note that an 'F382 ALU is used for the most significant package. Typical delays for *Figure a* are given in *Figure b*.

Fig. a 16-Bit Lookahead Carry ALU Expansion

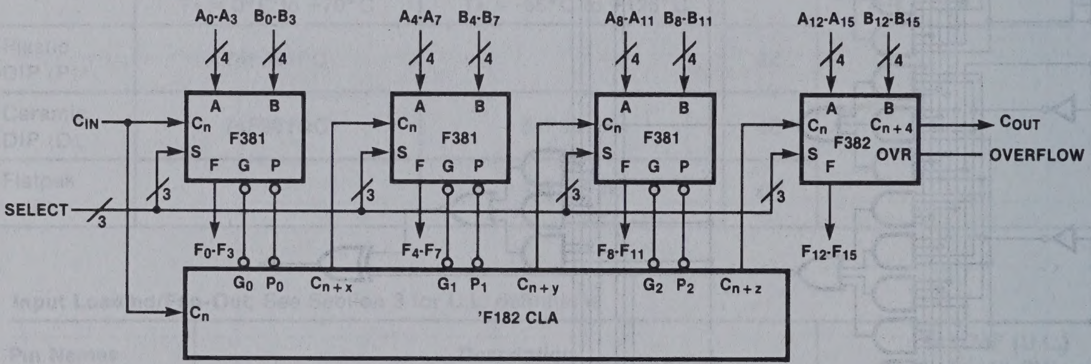

A0-A3
B0-B3
A4-A7
B4-B7
A8-A11
B8-B11
A12-A15
B12-B15
4
3
CIN
SELECT
A
B
Cn
S
F
G
P
F381
F382
Cn+4
OVR
COUT
OVERFLOW
F0-F3
F4-F7
F8-F11
F12-F15
G0
P0
Cn+x
G1
P1
Cn+y
G2
P2
Cn+z
'F182 CLA

Fig. b 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2 ns
$\overline{P}_i$ to C_{n+j} ('F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

Truth Table

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = HIGH Voltage Level
0 = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		59	89	mA	V_{CC} = Max, $S_0 - S_3$ = Gnd; Other Inputs HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	2.5 2.5	8.1 5.7	10.5 8.0	2.5 2.5	15 11.5	2.5 2.5	11.5 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	13.5 11	4.0 3.5	19 15.5	4.0 3.5	14.5 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to F_i	4.5 4.0	8.3 8.2	11 11	4.5 4.0	15.5 15.5	4.5 4.0	12 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{G}$	3.5 4.0	6.4 6.8	9.0 10	3.5 4.0	12.5 14	3.5 4.0	10 11	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{P}$	4.0 3.5	7.2 6.5	10.5 9.5	4.0 3.5	15 13	4.0 3.5	11.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to $\overline{G}$ or $\overline{P}$	4.0 4.5	7.8 10.2	10.5 13.5	4.0 4.5	15 19	4.0 4.5	11.5 14.5	ns	3-1 3-10

▨ Test limits in screened columns are preliminary.

54F/74F382

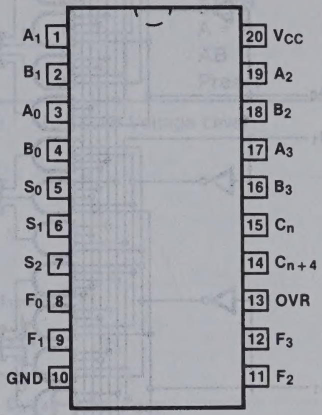
4-Bit Arithmetic Logic Unit

Description

The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the 'F381 data sheet.

- **Performs Six Arithmetic and Logic Functions**
- **Selectable Low (Clear) and High (Preset) Functions**
- **Low Input Loading Minimizes Drive Requirements**
- **Carry Output for Ripple Expansion**
- **Overflow Output for Twos Complement Arithmetic**

Connection Diagram


A1 1
B1 2
A0 3
B0 4
S0 5
S1 6
S2 7
F0 8
F1 9
GND 10
20 VCC
19 A2
18 B2
17 A3
16 B3
15 Cn
14 Cn+4
13 OVR
12 F3
11 F2

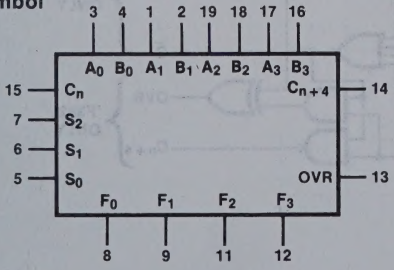
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F382PC		9Z
Ceramic DIP (D)	74F382DC	54F382DM	4E
Flatpak (F)		54F382FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

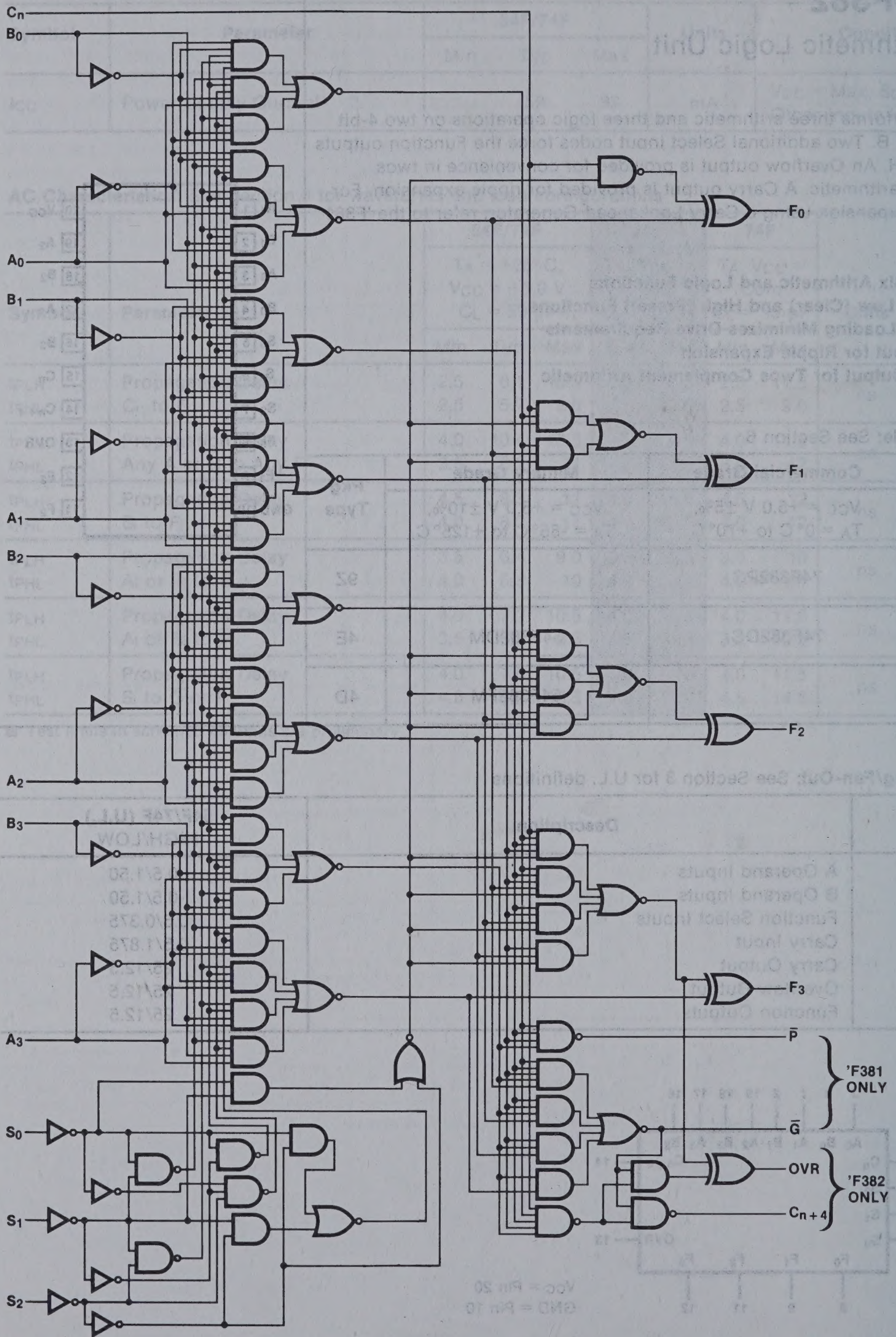
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	A Operand Inputs	0.5/1.50
$B_0 - B_3$	B Operand Inputs	0.5/1.50
$S_0 - S_2$	Function Select Inputs	0.5/0.375
C_n	Carry Input	0.5/1.875
C_{n+4}	Carry Output	25/12.5
OVR	Overflow Output	25/12.5
$F_0 - F_3$	Function Outputs	25/12.5

Logic Symbol


3
4
1
2
19
18
17
16
A0
B0
A1
B1
A2
B2
A3
B3
15
Cn
7
S2
6
S1
5
S0
Cn+4
14
OVR
13
F0
F1
F2
F3
8
9
11
12

V_{CC} = Pin 20
GND = Pin 10

Logic Diagram


Cn
B0
A0
B1
A1
B2
A2
B3
A3
S0
S1
S2
F0
F1
F2
F3
P̄
Ḡ
'F381 ONLY
OVR
Cn+4
'F382 ONLY

Functional Description

Signals applied to the Select inputs $S_0 - S_2$ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH operands, LOW for active-LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in *Figure a*. The Overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for *Figure a* are given in *Figure b*.

Function Table

SELECT			OPERATION
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level L = LOW Voltage Level

Fig. a 16-Bit Ripple Carry ALU Expansion

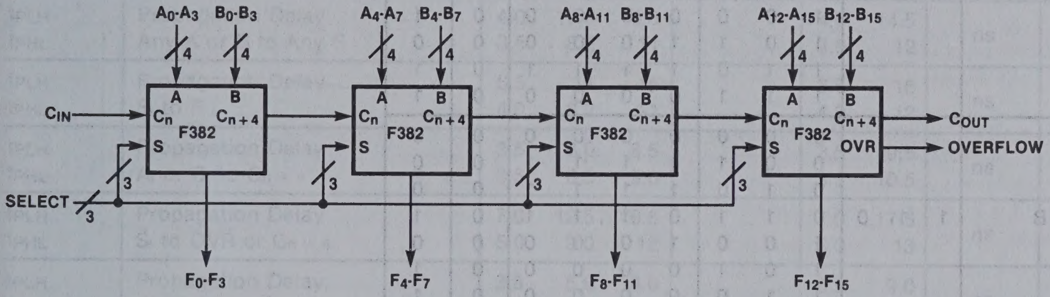


Fig. b 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

Truth Table

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	0	1
AB	0	1	1	X	0	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				X	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	X	0	0	1	1	1	1	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

1 = HIGH Voltage Level 0 = LOW Voltage Level X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		62	93	mA	V_{CC} = Max; S_0, C_n = HIGH Other Inputs Gnd

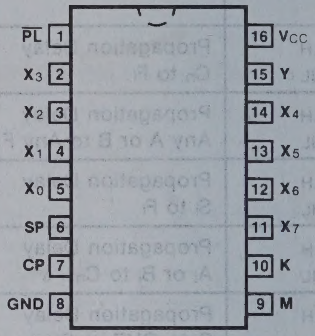
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	3.0 2.5	8.1 5.7	11.5 8.0			3.0 2.5	12.5 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	13.5 11			4.0 3.5	14.5 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to F_i	6.5 4.0	11 8.2	15 11			6.5 4.0	16 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to C_{n+4}	3.5 3.5	6.0 6.5	8.5 9.0			3.5 3.5	9.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to OVR or C_{n+4}	7.0 5.0	12.5 9.0	16.5 12			7.0 5.0	17.5 13	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	3.5 4.0	5.6 6.3	8.0 9.0			3.5 4.0	9.0 10	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_n to OVR	5.0 4.5	8.0 7.1	11 10			5.0 4.5	12 11	ns	3-1 3-10

54F/74F384

8-Bit Serial/Parallel Twos Complement Multiplier

Connection Diagram



Description

The 'F384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load ($\overline{PL}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

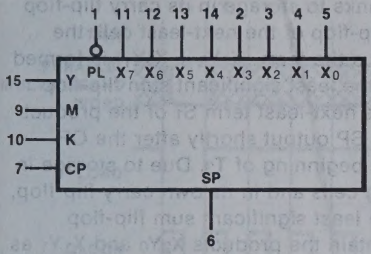
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0$ V ±5%, $T_A = 0°$C to +70°C	$V_{CC} = +5.0$ V ±10%, $T_A = -55°$C to +125°C	
Plastic DIP (P)	74F384PC		9B
Ceramic DIP (D)	74F384DC	54F384DM	6B
Flatpak (F)		54F384FM	4L

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
K	Serial Expansion Input	0.5/0.375
M	Mode Control Input	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.750
$X_0 - X_7$	Multiplicand Data Inputs	0.5/0.375
Y	Serial Multiplier Input	0.5/0.375
SP	Serial X • Y Product Output	25/12.5

Logic Symbol


1
11
12
13
14
3
2
4
5
PL
X7
X6
X5
X4
X3
X2
X1
X0
15
Y
9
M
10
K
7
CP
SP
6

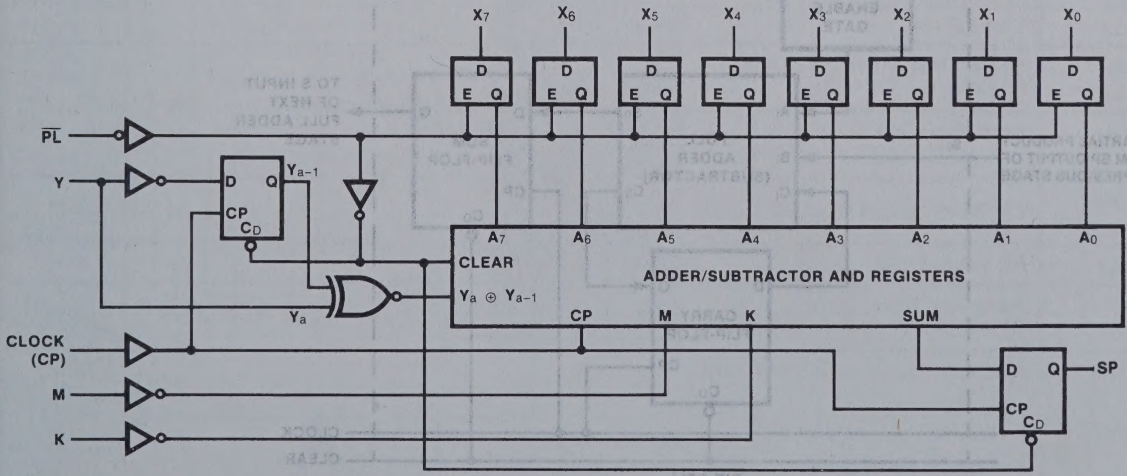
V_{CC} = Pin 16
GND = Pin 8

Function Table

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{PL}$	CP	K	M	X_i	Y	Y_{a-1}	SP	
		L	L					Most Significant Multiplier Device
		CS	H					Devices Cascaded in Multiplier String
L				OP		L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H								Device Enabled
H	↑				L	L	AR	Shift Sum Register
H					L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑				H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑				H	H	AR	Shift Sum Register

↑ = LOW-to-HIGH transition
CS = Connected to SP output of high order device
OP = X_i latches open for new data (i = 0.7)
AR = Output as required per Booth's algorithm

Logic Diagram


X7
X6
X5
X4
X3
X2
X1
X0
D
E Q
PL
Y
D
Q
Ya−1
CP
CD
Ya
CLOCK (CP)
M
K
A7
A6
A5
A4
A3
A2
A1
A0
CLEAR
Ya ⊕ Ya−1
ADDER/SUBTRACTOR AND REGISTERS
CP
M
K
SUM
D
Q
SP
CP
CD

Functional Description

Referring to the Logic Diagram, the multiplicand ($X_0 - X_7$) latches are enabled to receive new data when $\overline{PL}$ is LOW. Data that meet the setup time requirements are latched and stored when $\overline{PL}$ goes HIGH. The LOW signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. *Figure a* is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in lookahead carry schemes for longer words.

Figure b is a timing diagram for an 8 x 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input ($X_0 Y_0$) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package. The next-least bit Y_1 of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, thanks to storage in its carry flip-flop and in the sum flip-flop of the next-least cell, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. *Figure c* shows the method of using two 'F384s to perform a 12 x n bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to $X_4 - X_7$ of the most significant package. Whereas the 8 x 8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of *Figure c* requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

Fig. a Conceptual Carry Save Adder Cell

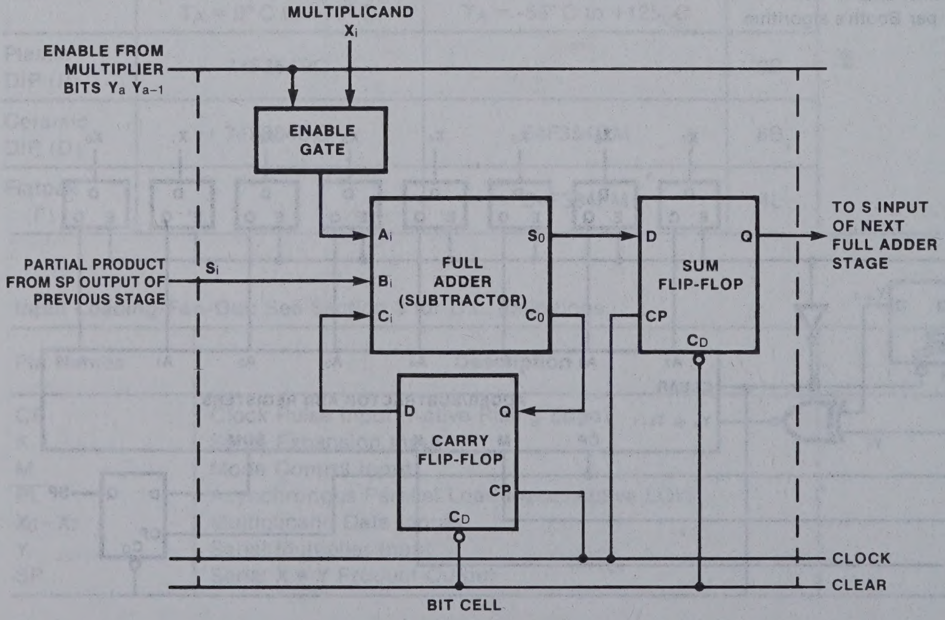


Fig. b Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication

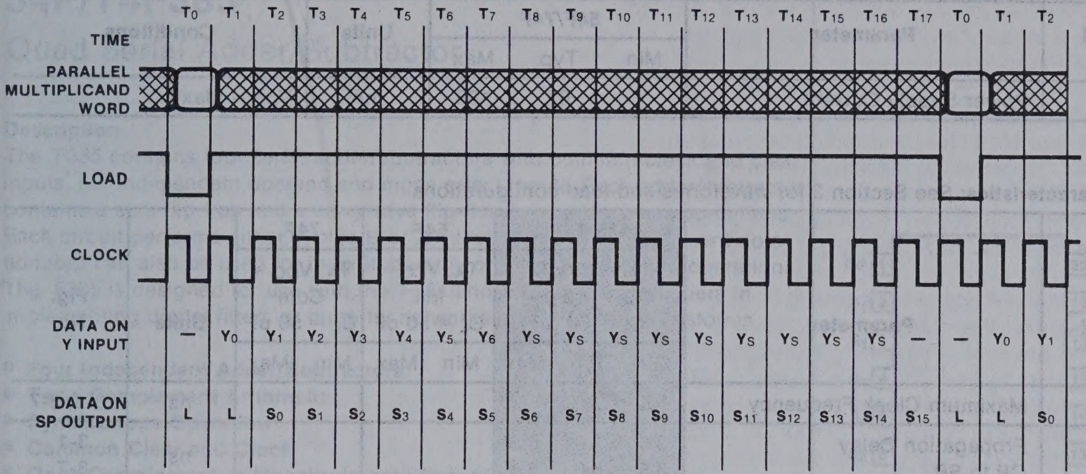
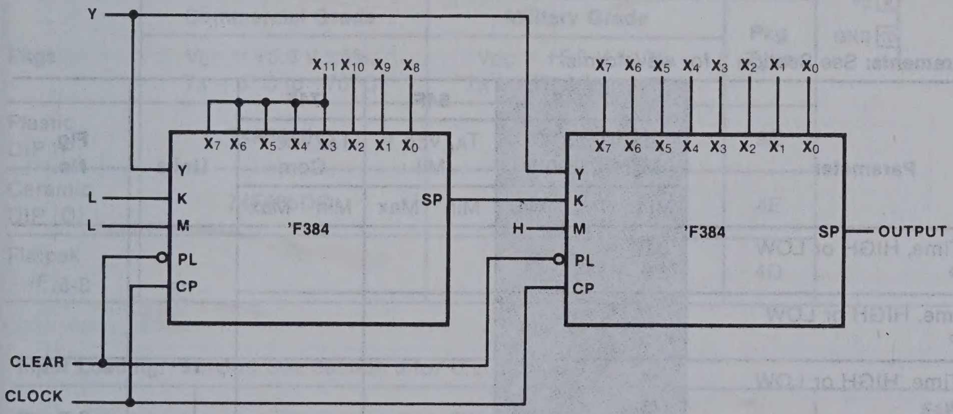

T_0 T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8 T_9 T_{10} T_{11} T_{12} T_{13} T_{14} T_{15} T_{16} T_{17} T_0 T_1 T_2
TIME
PARALLEL MULTIPLICAND WORD
LOAD
CLOCK
DATA ON Y INPUT
— Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_S Y_S Y_S Y_S Y_S Y_S Y_S Y_S Y_S — — Y_0 Y_1
DATA ON SP OUTPUT
L L S_0 S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10} S_{11} S_{12} S_{13} S_{14} S_{15} L L S_0

Fig. c 12-Bit by N-Bit Twos Complement Multiplier


Y
X_{11} X_{10} X_9 X_8
X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0
X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0
X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0
Y
K
M
PL
CP
L
L
'F384
SP
H
Y
K
M
PL
CP
'F384
SP
OUTPUT
CLEAR
CLOCK

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		67	108	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	100	70						ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to SP	3.5 3.5	6.0 6.0	8.5 8.5					ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{PL}$ to SP	4.0	7.0	10					ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V Min	Typ	Max	54F T_A, V_{CC} = Mil Min	Max	74F T_A, V_{CC} = Com Min	Max	Units	Fig. No.
t_s (H) t_s (L)	Setup Time, HIGH or LOW K to CP	8.0 8.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW K to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW Y to CP	15 15							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW Y to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW X_n to $\overline{PL}$	10 10							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW X_n to $\overline{PL}$	0 0								
t_w (H) t_w (L)	CP Width, HIGH or LOW	7.0 7.0							ns	3-7
t_w (L)	$\overline{PL}$ Width LOW	5.0							ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0							ns	3-11

■ Test limits in screened columns are preliminary.

54F/74F385

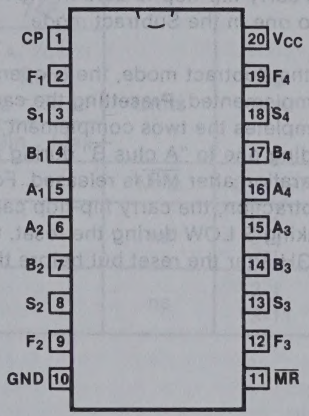
Quad Serial Adder/Subtractor

Description

The 'F385 contains four serial adder/subtractors with common clock and clear inputs, but independent operand and mode select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in twos complement notation, but can also be used for magnitude-only or ones complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

- **Four Independent Adder/Subtractors**
- **Twos Complement Arithmetic**
- **Synchronous Operation**
- **Common Clear and Clock**
- **Ones Complement or Magnitude-only Capability**

Connection Diagram



CP 1
F1 2
S1 3
B1 4
A1 5
A2 6
B2 7
S2 8
F2 9
GND 10
20 VCC
19 F4
18 S4
17 B4
16 A4
15 A3
14 B3
13 S3
12 F3
11 MR

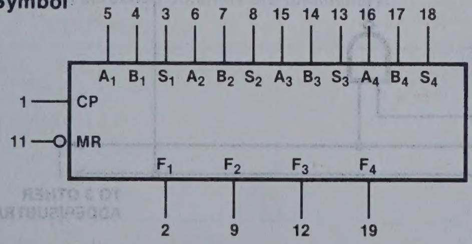
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F385PC		9Z
Ceramic DIP (D)	74F385DC	54F385DM	4E
Flatpak (F)		54F385FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_1 - A_4$	A Operand Inputs	0.5/0.375
$B_1 - B_4$	B Operand Inputs	0.5/0.375
$S_1 - S_4$	Function Select Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$F_1 - F_4$	Sum or Difference Outputs	25/12.5

Logic Symbol



5 4 3 6 7 8 15 14 13 16 17 18
A1 B1 S1 A2 B2 S2 A3 B3 S3 A4 B4 S4
1 CP
11 MR
F1 F2 F3 F4
2 9 12 19

VCC = Pin 20
GND = Pin 10

Functional Description

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset ($\overline{MR}$) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

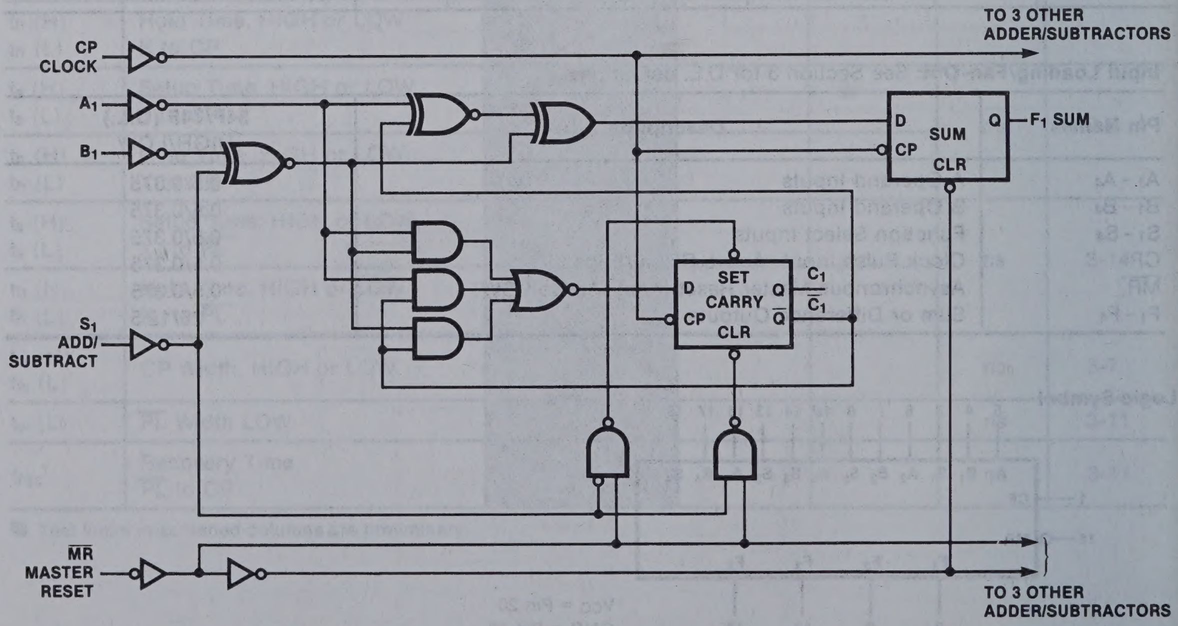
In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the twos complement transformation by adding one to "A plus $\overline{B}$" during the first (LSB) operation after $\overline{MR}$ is released. For ones complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

Truth Table

INPUTS*				INTERNAL CARRY		OUTPUT*	FUNCTION
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
* = Inputs before CP transition, output after C
C_1 = Carry flip-flop state before (C) and after (C_1) clock transition

Logic Diagram (one Adder/Subtractor shown)


TO 3 OTHER ADDER/SUBTRACTORS
CP CLOCK
A_1
B_1
D
Q
F_1 SUM
SUM
CP
CLR
SET
C_1
D
Q
CARRY
$\overline{C_1}$
$\overline{Q}$
CP
CLR
S_1 ADD/ SUBTRACT
$\overline{MR}$ MASTER RESET
TO 3 OTHER ADDER/SUBTRACTORS

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		68	104	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100						MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to F_n	3.0 3.0	6.0 6.0	8.5 8.5					ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to F_n	4.0	7.0	10					ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW B_n or S_n to CP	12 12							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW B_n or S_n to CP	0 0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	6.0 6.0							ns	3-7
t_w (L)	$\overline{MR}$ Width LOW	6.0							ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0							ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F398 • 54F/74F399

Quad 2-Port Register

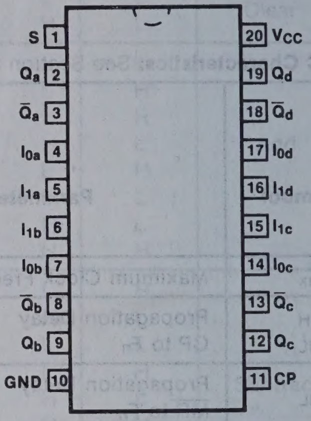
Description

The 'F398 and 'F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

- **Select Inputs from Two Data Sources**
- **Fully Positive Edge-triggered Operation**
- **Both True and Complement Outputs — 'F398**

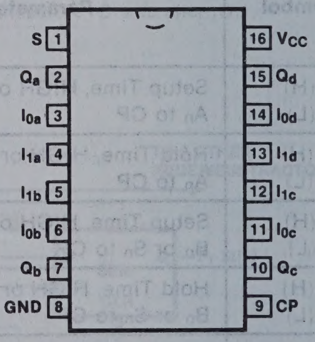
Connection Diagrams

'F398



S 1
Q_a 2
$\overline{Q}_a$ 3
I_{0a} 4
I_{1a} 5
I_{1b} 6
I_{0b} 7
$\overline{Q}_b$ 8
Q_b 9
GND 10
20 V_{CC}
19 Q_d
18 $\overline{Q}_d$
17 I_{0d}
16 I_{1d}
15 I_{1c}
14 I_{0c}
13 $\overline{Q}_c$
12 Q_c
11 CP

'F399



S 1
Q_a 2
I_{0a} 3
I_{1a} 4
I_{1b} 5
I_{0b} 6
Q_b 7
GND 8
16 V_{CC}
15 Q_d
14 I_{0d}
13 I_{1d}
12 I_{1c}
11 I_{0c}
10 Q_c
9 CP

Ordering Code: See Section 6

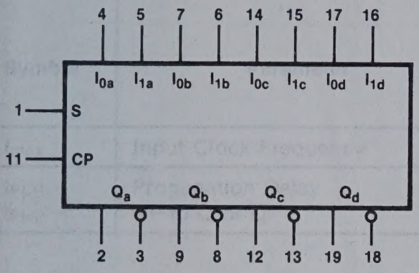
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F398PC 74F399PC		9Z 9B
Ceramic DIP (D)	74F398DC 74F399DC	54F398DM 54F399DM	4E 6B
Flatpak (F)		54F398FM 54F399FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S	Common Select Input	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5/0.375
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5/0.375
$Q_a - Q_d$	Register True Outputs	25/12.5
$\overline{Q}_a - \overline{Q}_d$	Register Complementary Outputs ('F398)	25/12.5

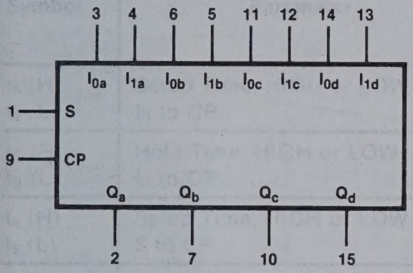
Logic Symbols

'F398


4
5
7
6
14
15
17
16
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
1
S
11
CP
Q_a
Q_b
Q_c
Q_d
2
3
9
8
12
13
19
18

V_{CC} = Pin 20
GND = Pin 10

'F399


3
4
6
5
11
12
14
13
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
1
S
9
CP
Q_a
Q_b
Q_c
Q_d
2
7
10
15

V_{CC} = Pin 16
GND = Pin 8

Functional Description

The 'F398 and 'F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

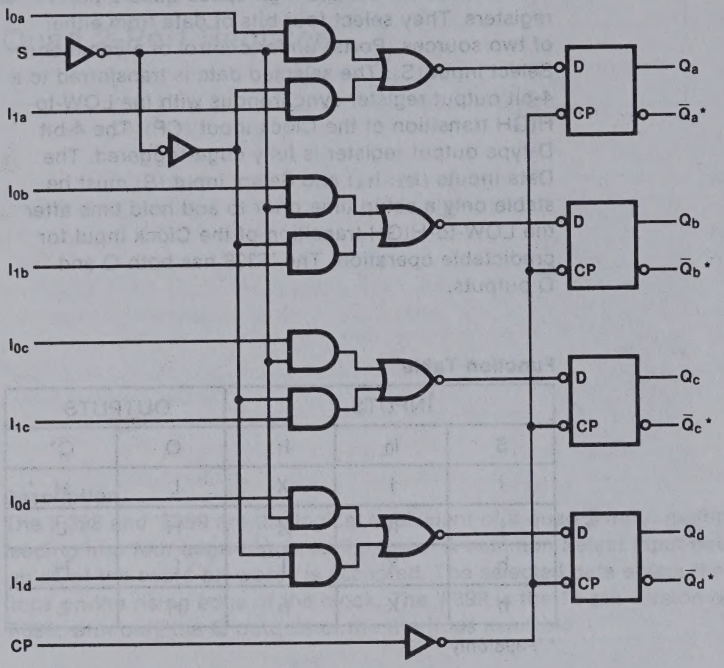
Function Table

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

* 'F398 only

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

Logic Diagram


I0a
S
I1a
I0b
I1b
I0c
I1c
I0d
I1d
CP
D
CP
Qa
Q̄a*
D
CP
Qb
Q̄b*
D
CP
Qc
Q̄c*
D
CP
Qd
Q̄d*

* 'F398 only

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current	'F398		25	38	mA	V_{CC} = Max, V_{IN} = GND CP = _⌐
		'F399		22	34		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Input Clock Frequency	100	140				100		MHz	3-1, 3-7
t_{PLH}	Propagation Delay CP to Q or $\overline{Q}$	3.5	6.0	8.0			3.5	9.0	ns	3-1
t_{PHL}		5.0	8.5	11			5.0	12		3-7

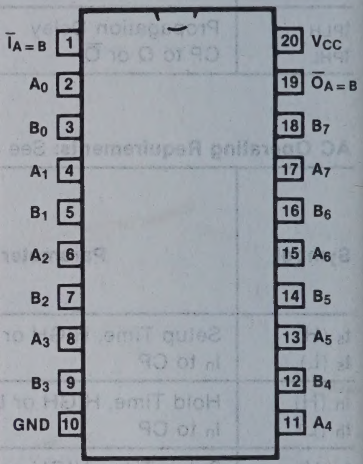
AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW I_n to CP	4.0					4.0		ns	3-1 3-5
t_s (L)		4.0					4.0			
t_h (H)	Hold Time, HIGH or LOW I_n to CP	1.0					1.0			
t_h (L)		1.0					1.0			
t_s (H)	Setup Time, HIGH or LOW S to CP	7.5					8.5		ns	3-5
t_s (L)		7.5					8.5			
t_h (H)	Hold Time, HIGH or LOW S to CP	0					0			
t_h (L)		0					0			
t_w (H)	Clock Pulse Width, HIGH or LOW	6.0					6.0		ns	3-7
t_w (L)		6.0					6.0			

54F/74F521

8-Bit Identity Comparator

Connection Diagram


$\overline{I}_{A=B}$ 1
A_0 2
B_0 3
A_1 4
B_1 5
A_2 6
B_2 7
A_3 8
B_3 9
GND 10
20 V_{CC}
19 $\overline{O}_{A=B}$
18 B_7
17 A_7
16 B_6
15 A_6
14 B_5
13 A_5
12 B_4
11 A_4

Description

The 'F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-LOW enable input.

- **Compares Two 8-Bit Words in 6.5 ns Typ**
- **Expandable to Any Word Length**
- **20-Pin Package**

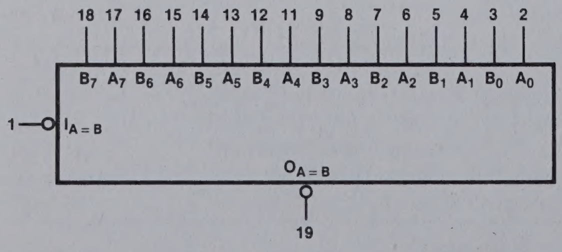
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C To +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F521PC		9Z
Ceramic DIP (D)	74F521DC	54F521DM	4E
Flatpak (F)		54F521FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_7$	Word A Inputs	0.5/0.375
$B_0 - B_7$	Word B Inputs	0.5/0.375
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)	0.5/0.375
$\overline{O}_{A=B}$	Identity Output (Active LOW)	25/12.5

Logic Symbol


18 17 16 15 14 13 12 11 9 8 7 6 5 4 3 2
B_7 A_7 B_6 A_6 B_5 A_5 B_4 A_4 B_3 A_3 B_2 A_2 B_1 A_1 B_0 A_0
1
$I_{A=B}$
$O_{A=B}$
19

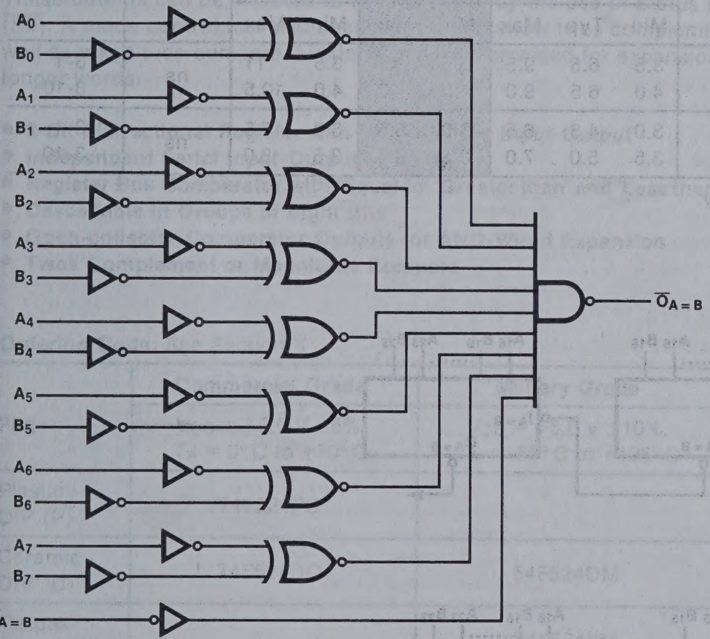
V_{CC} = Pin 20
GND = Pin 10

Truth Table

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram


A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
A = B
OA = B

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH} I_{CCL}	Power Supply Current		24 15.5	36 23	mA	V_{CC} = Max, $I_{A=B}$ = Gnd

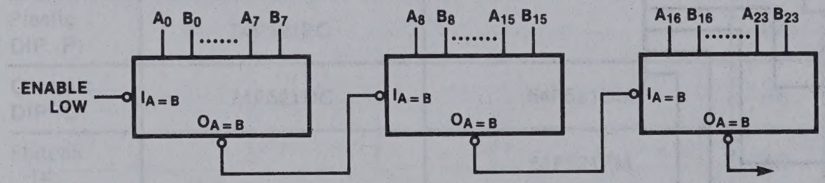
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F ▨		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			T_A, V_{CC} = Mil, $C_L = 50$ pF		T_A, V_{CC} = Com, $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.5 4.0	6.5 6.5	9.5 9.0	3.5 4.0	15 12	3.5 4.0	11 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.0 3.5	4.5 5.0	6.5 7.0	3.0 3.5	8.5 9.0	3.0 3.5	7.5 8.0	ns	3-1 3-10

▨ Test limits in screened columns are preliminary.

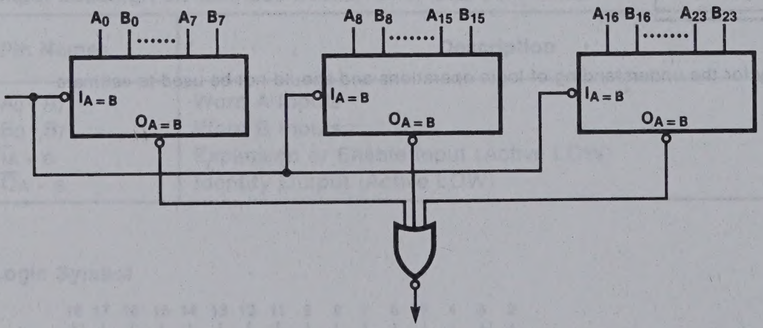
Applications

Ripple Expansion



A0 B0 ...... A7 B7
A8 B8 ...... A15 B15
A16 B16 ...... A23 B23
ENABLE LOW
IA=B
OA=B
IA=B
OA=B
IA=B
OA=B

Parallel Expansion



A0 B0 ...... A7 B7
A8 B8 ...... A15 B15
A16 B16 ...... A23 B23
IA=B
OA=B
IA=B
OA=B
IA=B
OA=B

54F/74F524

8-Bit Registered Comparator

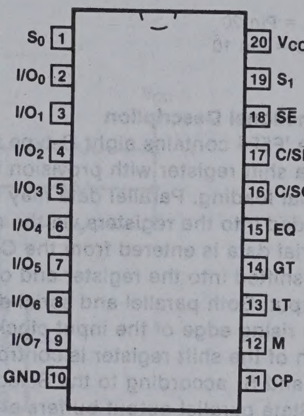
Description

The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow twos complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

- **8-Bit Bidirectional Register with Bus Oriented Input-Output**
- **Independent Serial Input-Output to Register**
- **Register Bus Comparator with 'Equal to' 'Greater than' and 'Less than' Outputs**
- **Cascadable in Groups of Eight Bits**
- **Open-collector Comparator Outputs for AND-Wired Expansion**
- **Twos Complement or Magnitude Compare**

Connection Diagram



Ordering Code: See Section 6

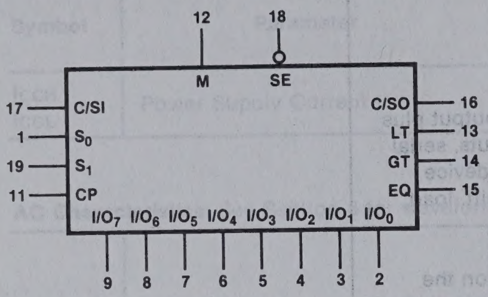
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F524PC		9Z
Ceramic DIP (D)	74F524DC	54F524DM	4E
Flatpak (F)		54F524FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	0.5/0.375
C/SI	Status Priority or Serial Data Input	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{SE}$	Status Enable Input (Active LOW)	0.5/0.375
M	Compare Mode Select Input	0.5/0.375
I/O_0 - I/O_7	Parallel Data Inputs or 3-State Parallel Data Outputs	1.25/0.375 25/12.5
C/SO	Status Priority or Serial Data Output	25/12.5
LT	Register Less Than Bus Output	OC*/12.5
EQ	Register Equal Bus Output	OC*/12.5
GT	Register Greater Than Bus Output	OC*/12.5

*OC = Open Collector

Logic Symbol


12
18
M
SE
17
C/SI
1
S_0
19
S_1
11
CP
C/SO
16
LT
13
GT
14
EQ
15
I/O_7 I/O_6 I/O_5 I/O_4 I/O_3 I/O_2 I/O_1 I/O_0
9 8 7 6 5 4 3 2

V_{CC} = Pin 20
GND = Pin 10

Functional Description

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus $I/O_0 - I/O_7$. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals S_0 and S_1 according to the Select Truth Table. The 3-State parallel output buffers are enabled only in the Read mode.

Select Truth Table

S_0	S_1	OPERATION
L	L	HOLD — Retains data in shift register
L	H	READ — Read contents in register onto data bus
H	L	SHIFT — Allows serial shifting on next rising clock edge
H	H	LOAD — Load data on bus into register

H = HIGH Voltage Level
L = LOW Voltage Level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

Number Representation Select Table

M	OPERATION
L	Magnitude compare
H	Twos complement compare

H = HIGH Voltage Level
L = LOW Voltage Level

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word length greater than eight bits.

Status Truth Table (Hold Mode)

INPUTS			OUTPUTS			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	①
L	L	$O_A - O_H > I/O_0 - I/O_7$	L	H	H	L
L	L	$O_A - O_H = I/O_0 - I/O_7$	H	H	H	H
L	L	$O_A - O_H < I/O_0 - I/O_7$	L	H	H	L
L	H	$O_A - O_H > I/O_0 - I/O_7$	L	H	L	L
L	H	$O_A - O_H = I/O_0 - I/O_7$	H	L	L	H
L	H	$O_A - O_H < I/O_0 - I/O_7$	L	L	H	L

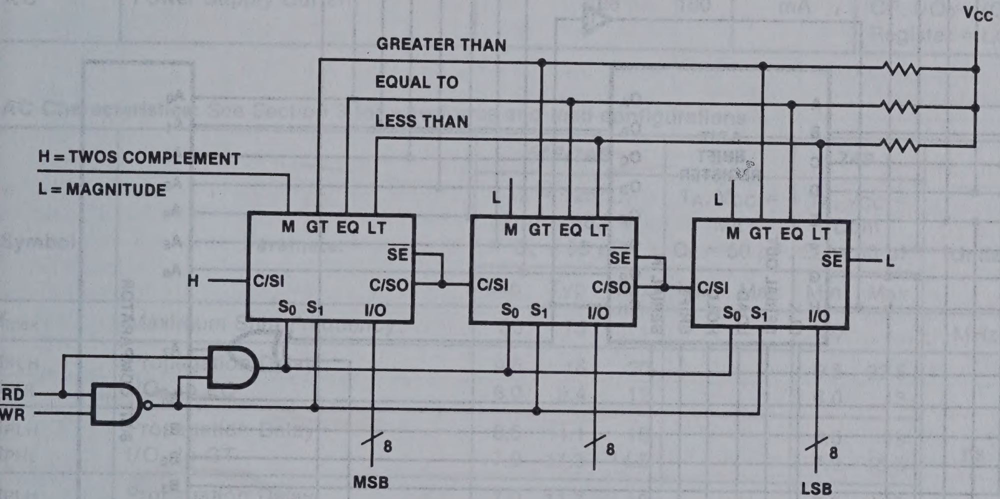
① = HIGH if data are equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see *Figure a*). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

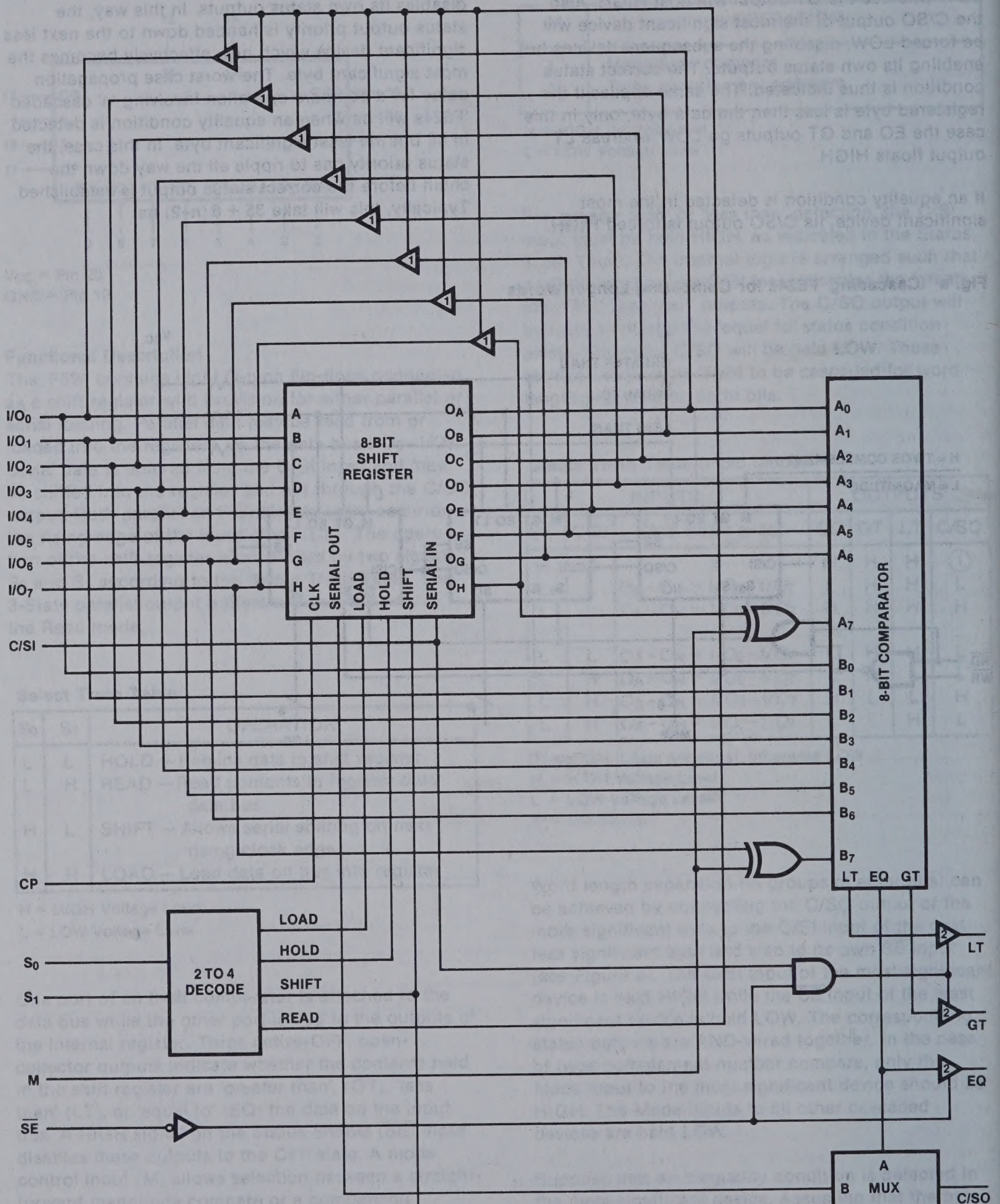
Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled LOW whereas the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW whereas LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6 (n–2) ns.

Fig. a Cascading 'F524s for Comparing Longer Words


GREATER THAN
EQUAL TO
LESS THAN
VCC
H = TWOS COMPLEMENT
L = MAGNITUDE
L
L
M GT EQ LT
SE
C/SI
C/SO
S0 S1
I/O
H
M GT EQ LT
SE
C/SI
C/SO
S0 S1
I/O
M GT EQ LT
SE
L
C/SI
S0 S1
I/O
RD
WR
8
MSB
8
8
LSB

Functional Block Diagram


I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
C/SI
CP
S_0
S_1
M
$\overline{SE}$
1
A
B
C
D
E
F
G
H
8-BIT SHIFT REGISTER
O_A
O_B
O_C
O_D
O_E
O_F
O_G
O_H
CLK
SERIAL OUT
LOAD
HOLD
SHIFT
SERIAL IN
2 TO 4 DECODE
LOAD
HOLD
SHIFT
READ
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
B_0
B_1
B_2
B_3
B_4
B_5
B_6
B_7
8-BIT COMPARATOR
LT EQ GT
2
LT
GT
EQ
A
B MUX
S
C/SO

Notes
1. 3-State Output
2. Open-Collector Output

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{IH}	Input HIGH Current Breakdown Test, $I/O_0 - I/O_7$			1.0	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{OH}	Output HIGH Current GT, EQ, LT			-100	µA	V_{CC} = Min, V_{OUT} = 4.5 V
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, $I/O_0 - I/O_7$			70	µA	V_{CC} = Max, V_{OUT} = 2.4 V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, $I/O_0 - I/O_7$			600	µA	V_{CC} = Max, V_{IN} = 0.5 V
I_{CC}	Power Supply Current		128	180	mA	S_0, S_1, $\overline{SE}$, C/SI = 4.5 V CP, $I/O_0 - I/O_7$, Register = LOW

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Maximum Shift Frequency	50	75				50		MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay I/O_n to EQ	9.5 6.0	16 9.4	20 12			9.5 6.0	22.5 13	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I/O_n to GT	8.5 7.0	14.1 11.3	18 14.5			8.5 7.0	19 15.5		
t_{PLH} t_{PHL}	Propagation Delay I/O_n to LT	7.0 6.0	11.7 10.2	16 14			7.0 6.0	18 15		
t_{PLH} $_{PHL}$	Propagation Delay I/O_n to C/SO	9.0 6.0	15.2 10.4	19.5 13			9.0 6.0	21.5 14	ns	3-1 3-10
$_{PLH}$ $_{PHL}$	Propagation Delay CP to EQ	10.5 4.0	17.5 7.0	22 9.0			10.5 3.5	24.5 10	ns	3-1 3-7
$_{PLH}$ $_{PHL}$	Propagation Delay CP to GT	10 9.0	16.5 15.3	21 20			10 9.0	22 21.5		
$_{PLH}$ $_{PHL}$	Propagation Delay CP to LT	9.0 6.0	15.5 9.6	19.5 12.5			9.0 6.0	21 13.5		
$_{PLH}$	Propagation Delay CP to C/SO (Compare)	8.5	14.5	18.5			8.5	21.5	ns	3-1 3-7
$_{PLH}$ $_{PHL}$	Propagation Delay CP to C/SO (Serial Shift)	5.0 5.0	8.3 7.6	10.5 10			5.0 5.0	11.5 11		
$_{PLH}$ $_{PHL}$	Propagation Delay C/SI to GT	9.0 3.5	14.9 6.5	19 8.5			9.0 3.0	20 9.5	ns	3-1 3-3
$_{PLH}$ $_{PHL}$	Propagation Delay C/SI to LT	8.0 4.0	13.5 6.5	17 8.5			8.0 4.0	18 9.5		

AC Characteristics (Cont'd): See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_0, S_1 to C/SO	7.0	11.3	14.5			7.0	15.5	ns	3-1 3-10
t_{PHL}		6.0	9.3	12			6.0	13		
t_{PLH}	Propagation Delay $\overline{SE}$ to EQ	4.0	6.3	8.0			4.0	9.0	ns	3-1 3-4
t_{PHL}		2.5	4.6	6.0			2.5	6.5		
t_{PLH}	Propagation Delay $\overline{SE}$ to GT	7.5	12.5	16			7.5	17		
t_{PHL}		3.5	6.5	8.0			3.5	9.0		
t_{PLH}	Propagation Delay $\overline{SE}$ to LT	5.0	8.5	11			5.0	12	ns	3-1 3-4
t_{PHL}		3.5	6.2	8.0			3.5	9.0		
t_{PLH}	Propagation Delay C/SI to C/SO	4.5	7.4	9.5			4.5	10.5	ns	3-1 3-4
t_{PHL}		4.0	7.3	9.5			4.0	10.5		
t_{PLH}	Propagation Delay M to GT	8.0	13.4	17			8.0	18	ns	3-1 3-10
t_{PHL}		7.0	12.1	15.5			7.0	17		
t_{PLH}	Propagation Delay M to LT	8.5	14.4	19			8.5	21		
t_{PHL}		5.5	9.4	12			5.5	13		
t_{PZH}	Output Enable Time S_0, S_1 to I/O_n	6.0	10.1	13			6.0	14	ns	3-1 3-12 3-13
t_{PZL}		6.5	11.2	14.5			6.5	15.5		
t_{PHZ}	Output Disable Time S_0, S_1 to I/O_n	5.0	7.9	10			5.0	11		
t_{PLZ}		5.5	9.6	12.5			5.5	13.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW I/O_n to CP	5.0					5.0		ns	3-5
t_s (L)		5.0					5.0			
t_h (H)	Hold Time, HIGH or LOW I/O_n to CP	0					0			
t_h (L)		0					0			
t_s (H)	Setup Time, HIGH or LOW S_0, S_1 to CP	10					10		ns	3-5
t_s (L)		10					10			
t_s (H)	Setup Time, HIGH or LOW C/SI to CP	5.0					5.0		ns	3-5
t_s (L)		7.0					7.0			
t_h (H)	Hold Time, HIGH or LOW C/SI to CP	0					0			
t_h (L)		0					0			
t_w (H)	Clock Pulse Width HIGH	4.0					4.0		ns	3-7

54F/74F533

Octal Transparent Latch

(With 3-State Outputs)

Description

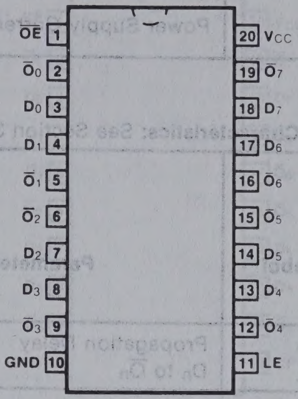
The 'F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state. The 'F533 is the same as the 'F373, except that the outputs are inverted. For description and logic diagram please see the 'F373 data sheet.

- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

Ordering Code: See Section 6

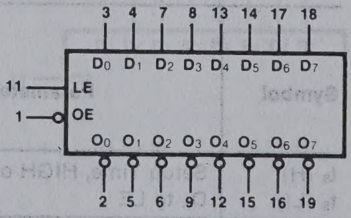
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F533PC		9Z
Ceramic DIP (D)	74F533DC	54F533DM	4E
Flatpak (F)		54F533FM	4D

Connection Diagram



OE 1
Ō0 2
D0 3
D1 4
Ō1 5
Ō2 6
D2 7
D3 8
Ō3 9
GND 10
20 VCC
19 Ō7
18 D7
17 D6
16 Ō6
15 Ō5
14 D5
13 D4
12 Ō4
11 LE

Logic Symbol



3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 LE
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
2 5 6 9 12 15 16 19

V_{CC} = Pin 20
GND = Pin 10

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0 - \overline{O}_7$	Complementary 3-State Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current		41	61	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	12 9.0	4.0 3.0	10 8.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0 3.0	8.5 5.6	11 7.0	5.0 3.0	14 9.0	5.0 3.0	13 8.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	7.7 5.1	10 6.5	2.0 2.0	12.5 9.0	2.0 2.0	11 7.5	ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	8.5 7.5	2.0 2.0	7.0 6.5	ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

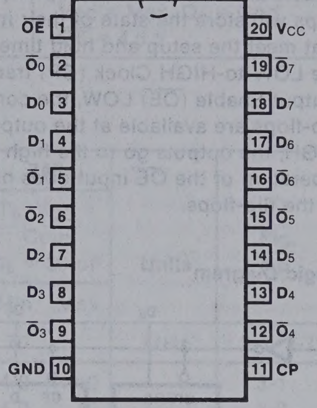
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0			2.0 2.0		2.0 2.0		ns	3-15
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-15
t_w (H)	LE Pulse Width HIGH	6.0			6.0		6.0		ns	3-7

54F/74F534

Octal D-Type Flip-Flop

(With 3-State Outputs)

Connection Diagram


$\overline{OE}$ 1
$\overline{O}_0$ 2
D_0 3
D_1 4
$\overline{O}_1$ 5
$\overline{O}_2$ 6
D_2 7
D_3 8
$\overline{O}_3$ 9
GND 10
11 CP
12 $\overline{O}_4$
13 D_4
14 D_5
15 $\overline{O}_5$
16 $\overline{O}_6$
17 D_6
18 D_7
19 $\overline{O}_7$
20 V_{CC}

Description

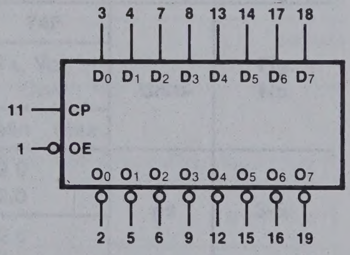
The 'F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-triggered Clock**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F534PC		9Z
Ceramic DIP (D)	74F534DC	54F534DM	4E
Flatpak (F)		54F534FM	4D

Logic Symbol


3
4
7
8
13
14
17
18
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
11 CP
1 OE
O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7
2
5
6
9
12
15
16
19

V_{CC} = Pin 20
GND = Pin 10

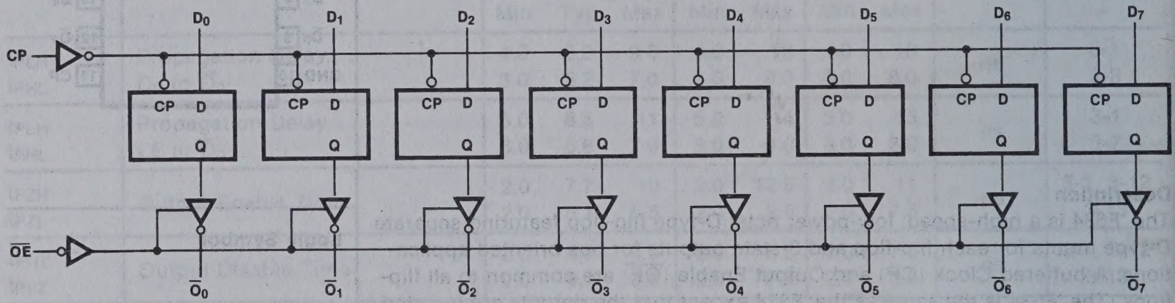
Input Loading/Fan-Out: See Section 3 for U.L. definitons

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
D_0 - D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0$ - $\overline{O}_7$	Complementary 3-State Outputs	25/12.5

Functional Description

The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100			60		70		MHz	3-1, 3-7
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	4.0	6.5	8.5	4.0	10.5	4.0	10	ns	3-1 3-7
t_{PHL}		4.0	6.5	8.5	4.0	11	4.0	10		
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14	2.0	12.5	ns	3-1 3-12 3-13
t_{PZL}		2.0	5.8	7.5	2.0	10	2.0	8.5		
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0		
t_{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5		

AC Operating Requirements: See Section 3 for waveforms

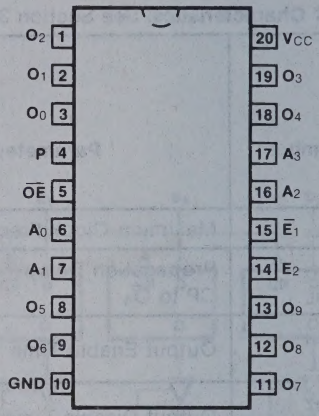
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW D_n to CP	2.0			2.5		2.0		ns	3-5
t_s (L)		2.0			2.0		2.0			
t_h (H)	Hold Time, HIGH or LOW D_n to CP	2.0			2.0		2.0			
t_h (L)		2.0			2.5		2.0			
t_w (H)	CP Pulse Width, HIGH or LOW	7.0			7.0		7.0		ns	3-7
t_w (L)		6.0			6.0		6.0			

▨ Test limits in screened columns are preliminary.

54F/74F537

1-of-10 Decoder
(With 3-State Outputs)

Connection Diagram


O2 1
O1 2
O0 3
P 4
OE 5
A0 6
A1 7
O5 8
O6 9
GND 10
20 VCC
19 O3
18 O4
17 A3
16 A2
15 E1
14 E2
13 O9
12 O8
11 O7

Description

The 'F537 is a one-of-ten decoder/demultiplexer with four active-HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high-impedance state. Two input enables, active-HIGH E_2 and active-LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

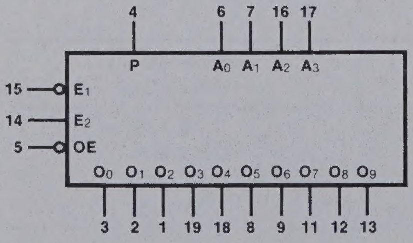
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F537PC		9Z
Ceramic DIP (D)	74F537DC	54F537DM	4E
Flatpak (F)		54F537FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.375
E_2	Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
P	Polarity Control Input	0.5/0.375
$O_0 - O_9$	3-State Outputs	25/12.5

Logic Symbol


4
6
7
16
17
P
A0
A1
A2
A3
15
E1
14
E2
5
OE
O0 O1 O2 O3 O4 O5 O6 O7 O8 O9
3 2 1 19 18 8 9 11 12 13

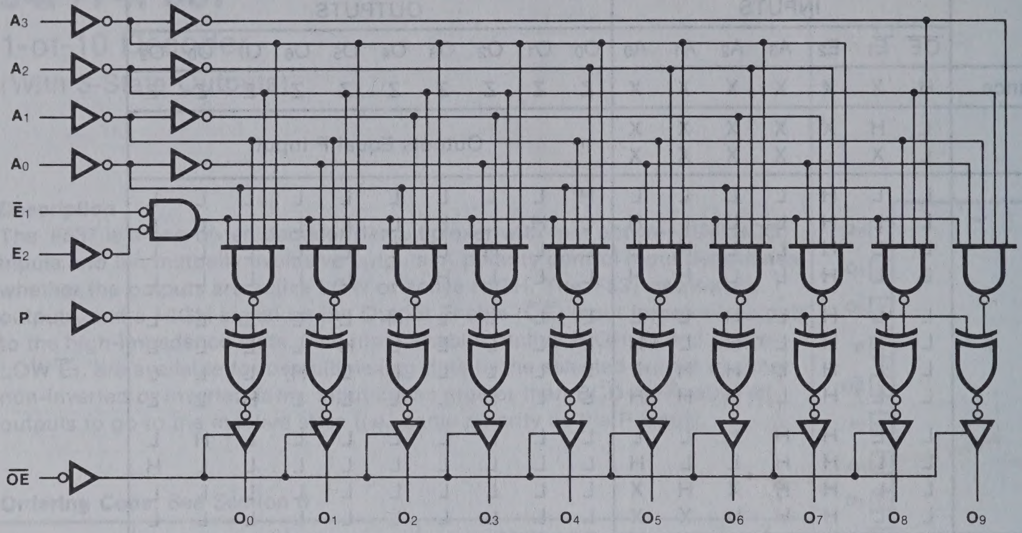
V_{CC} = Pin 20
GND = Pin 10

Truth Table

FUNCTION	INPUTS							OUTPUTS									
	$\overline{OE}$	$\overline{E}_1$	E_2	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	X	X	X	X	Outputs Equal P Input									
	L	X	L	X	X	X	X										
Active-HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L
Active-LOW Output (P = H)	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CCZ}	Power Supply Current		44	66	mA	$A_0 - A_3$, $\overline{E}_1$ = Gnd $\overline{OE}$, E_2, P = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

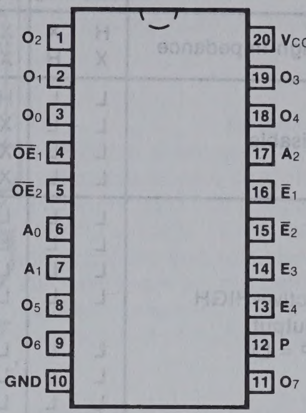
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			T_A, V_{CC} = Mil, $C_L = 50$ pF		T_A, V_{CC} = Com, $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	6.0	11	16			6.0	17	ns	3-1 3-10
t_{PHL}	A_n to O_n	4.0	7.5	11			4.0	12		
t_{PLH}	Propagation Delay	5.0	8.5	12			5.0	13		
t_{PHL}	$\overline{E}_1$ to O_n	4.0	6.5	9.0			4.0	10		
t_{PLH}	Propagation Delay	6.0	11	16			6.0	17	ns	3-1 3-10
t_{PHL}	E_2 to O_n	5.0	10	14			5.0	15		
t_{PLH}	Propagation Delay	6.0	11.5	16			6.0	17		
t_{PHL}	P to O_n	6.0	11	16			6.0	17		
t_{PZH}	Output Enable Time	3.0	5.5	8.0			3.0	9.0	ns	3-1 3-12 3-13
t_{PZL}	$\overline{OE}$ to O_n	5.0	9.0	13			5.0	14		
t_{PHZ}	Output Disable Time	2.0	4.0	6.0			2.0	7.0		
t_{PLZ}	$\overline{OE}$ to O_n	3.0	5.0	7.0			3.0	8.0		

54F/74F538

1-of-8 Decoder

(With 3-State Outputs)

Connection Diagram



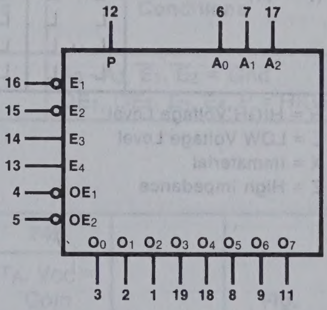
O2 1
O1 2
O0 3
OE1 4
OE2 5
A0 6
A1 7
O5 8
O6 9
GND 10
20 VCC
19 O3
18 O4
17 A2
16 Ē1
15 Ē2
14 E3
13 E4
12 P
11 O7

Description

The 'F538 decoder/demultiplexer accepts three Address ($A_0 - A_2$) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH signal on either of the active-LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high-impedance state. Two active-HIGH and two active-LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to one-of-eight or one-of-16 destinations.

- **Output Polarity Control**
- **Data Demultiplexing Capability**
- **Multiple Enables for Expansion**
- **3-State Outputs**

Logic Symbol



12
6
7
17
P
A0
A1
A2
16
15
14
13
4
5
E1
E2
E3
E4
OE1
OE2
O0
O1
O2
O3
O4
O5
O6
O7
3
2
1
19
18
8
9
11

VCC = Pin 20
GND = Pin 10

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F538PC		9Z
Ceramic DIP (D)	74F538DC	54F538DM	4E
Flatpak (F)		54F538FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

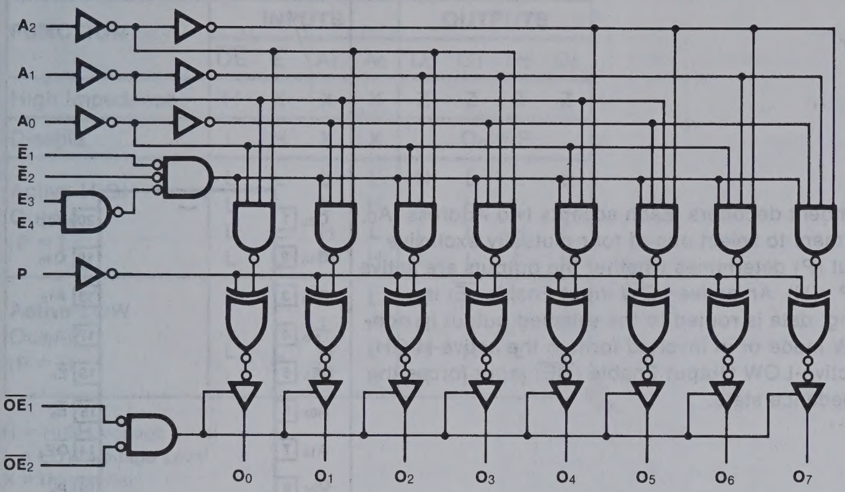
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Enable Inputs (Active HIGH)	0.5/0.375
P	Polarity Control Input	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)	0.5/0.375
$O_0 - O_7$	3-State Outputs	25/12.5

Truth Table

FUNCTION	INPUTS									OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active-HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current		37	56	mA	$A_0 - A_2$, $\overline{E}_1$, $\overline{E}_2$ = Gnd $\overline{OE}_1$, $\overline{OE}_2$, E_3, E_4, P = HIGH

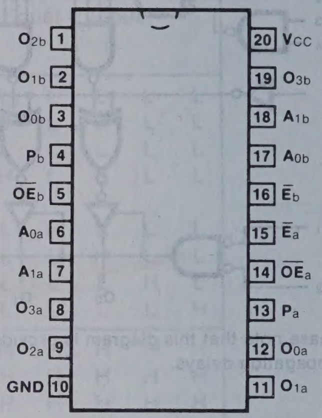
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	6.0 4.0	11 7.5	16 11			6.0 4.0	17 12	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to O_n	5.0 4.0	8.5 6.5	12 9.0			5.0 4.0	13 10		
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to O_n	6.0 5.0	11 10	16 14			6.0 5.0	17 15	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay P to O_n	6.0 6.0	11.5 11	16 16			6.0 6.0	17 17		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	3.0 5.0	5.5 9.0	8.0 13			3.0 5.0	9.0 14	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	2.0 3.0	4.0 5.0	6.0 9.0			2.0 3.0	7.0 8.0		

54F/74F539

Dual 1-of-4 Decoder
(With 3-State Outputs)

Connection Diagram


O_{2b} 1
O_{1b} 2
O_{0b} 3
P_b 4
$\overline{OE}_b$ 5
A_{0a} 6
A_{1a} 7
O_{3a} 8
O_{2a} 9
GND 10
20 V_{CC}
19 O_{3b}
18 A_{1b}
17 A_{0b}
16 $\overline{E}_b$
15 $\overline{E}_a$
14 $\overline{OE}_a$
13 P_a
12 O_{0a}
11 O_{1a}

Description

The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH (P = L) or active LOW (P = H). An active-LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active-LOW mode or in inverted form in the active-HIGH mode. A HIGH signal on the active-LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

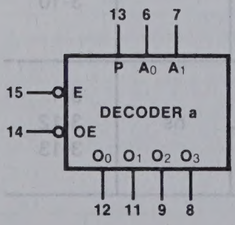
Ordering Code: See Section 6

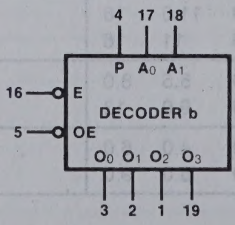
Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F539PC		9Z
Ceramic DIP (D)	74F539DC	54F539DM	4E
Flatpak (F)		54F539FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
A_{0a} - A_{1a}	Side A Address Inputs	0.5/0.375
A_{0b} - A_{1b}	Side B Address Inputs	0.5/0.375
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	0.5/0.375
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable Inputs (Active LOW)	0.5/0.375
P_a, P_b	Polarity Control Inputs	0.5/0.375
O_{0a} - O_{3a}	Side A 3-State Outputs	25/12.5
O_{0b} - O_{3b}	Side B 3-State Outputs	25/12.5

Logic Symbol


13
6
7
P
A_0
A_1
15
E
DECODER a
14
OE
O_0
O_1
O_2
O_3
12
11
9
8


4
17
18
P
A_0
A_1
16
E
DECODER b
5
OE
O_0
O_1
O_2
O_3
3
2
1
19

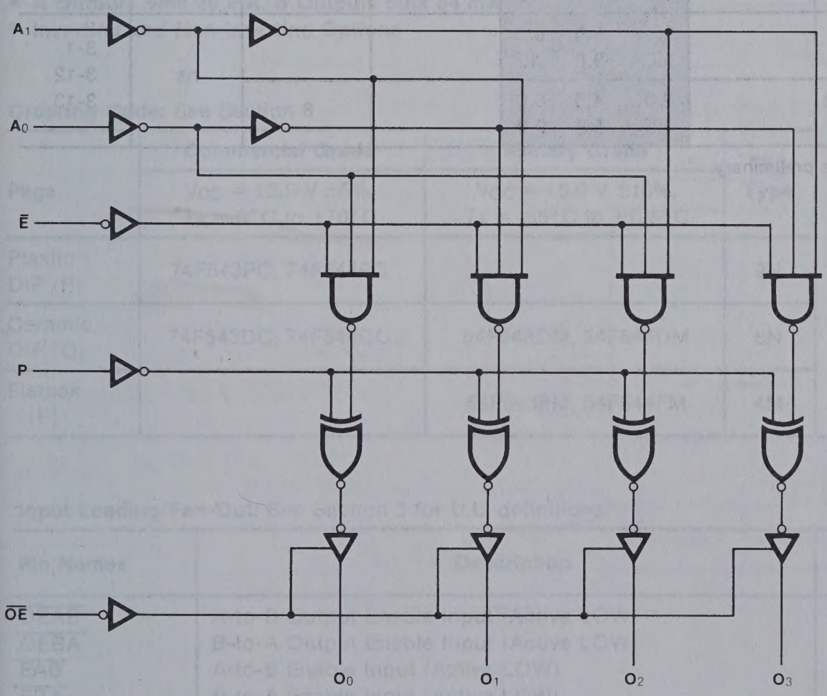
V_{CC} = Pin 20
GND = Pin 10

Truth Table (each half)

FUNCTION	INPUTS				OUTPUTS			
	$\overline{OE}$	$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active-HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active-LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		41	62	mA	A_0, A_1, $\overline{E}$ = Gnd $\overline{OE}$, P = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	6.0 4.0	11.6 7.5	16 11					ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to O_n	6.0 5.0	11 10	16 14					ns	3-1 3-10
t_{PLH} t_{PHL}	Progagation Delay P to O_n	6.0 6.0	11.5 11	16 16					ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.0 5.0	5.5 9.0	8.0 13					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0 3.0	4.0 5.0	6.0 9.0						

▨ Test limits in screened columns are preliminary.

54F/74F543 • 54F/74F544

Octal Registered Transceiver

Description

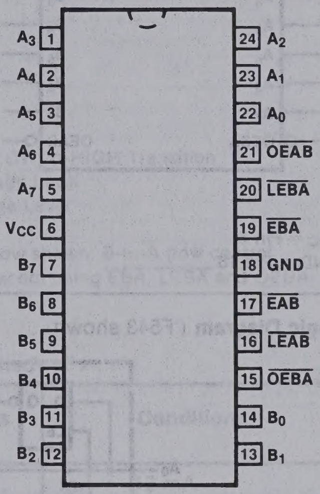
The 'F543 and 'F544 octal transceivers each contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA. The 'F543 is non-inverting; the 'F544 inverts data in both directions.

- **8-Bit Octal Transceiver**
- **Back-to-Back Registers for Storage**
- **Separate Controls for Data Flow in Each Direction**
- **A Outputs Sink 20 mA, B Outputs Sink 64 mA**
- **Inverting and Non-inverting Options**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F543PC, 74F544PC		9N
Ceramic DIP (D)	74F543DC, 74F544DC	54F543DM, 54F544DM	6N
Flatpak (F)		54F543FM, 54F544FM	4M

Connection Diagram
('F543 shown*)



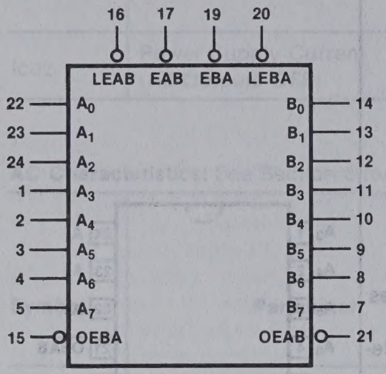
*'F544 has inverting outputs

Input Loading/Fan-Out: See Section 3 for U.L. definitions

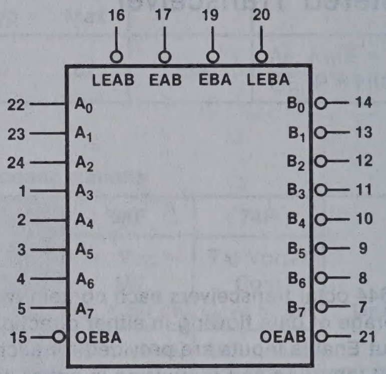
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	0.5/0.375
$\overline{EAB}$	A-to-B Enable Input (Active LOW)	0.5/0.375
$\overline{EBA}$	B-to-A Enable Input (Active LOW)	0.5/0.375
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	0.5/0.375
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	0.5/0.375
$A_0 - A_7$	A-to-B Data Inputs or B-to-A 3-State Outputs	1.75/0.375 25/12
$B_0 - B_7$	B-to-A Data Inputs or A-to-B 3-State Outputs	1.75/0.375 25/40 (30)

Logic Symbols

'F543

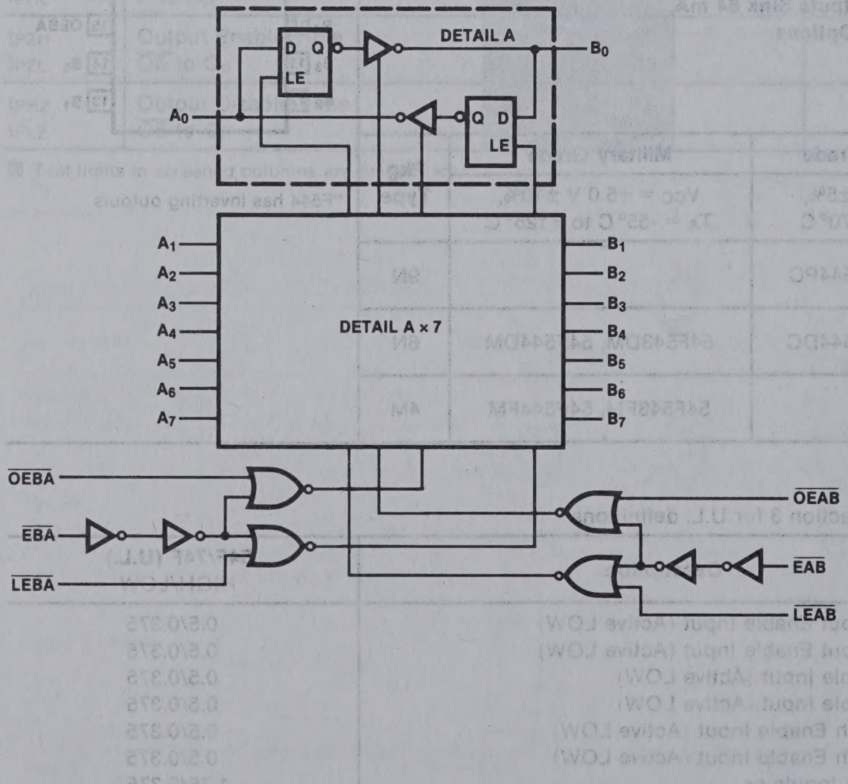

16
17
19
20
LEAB
EAB
EBA
LEBA
22 A0
23 A1
24 A2
1 A3
2 A4
3 A5
4 A6
5 A7
15 OEBA
B0 14
B1 13
B2 12
B3 11
B4 10
B5 9
B6 8
B7 7
OEAB 21

'F544


16
17
19
20
LEAB
EAB
EBA
LEBA
22 A0
23 A1
24 A2
1 A3
2 A4
3 A5
4 A6
5 A7
15 OEBA
B0 14
B1 13
B2 12
B3 11
B4 10
B5 9
B6 8
B7 7
OEAB 21

V_{CC} = Pin 6
GND = Pin 18

Logic Diagram ('F543 shown)


DETAIL A
D Q
LE
Q D
LE
A0
B0
A1
A2
A3
A4
A5
A6
A7
DETAIL A × 7
B1
B2
B3
B4
B5
B6
B7
OEBA
EBA
LEBA
OEAB
EAB
LEAB

Functional Description

The 'F543 and 'F544 each contain two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\mathrm{EAB}}$) input must be LOW in order to enter data from $A_0 - A_7$ or take data from $B_0 - B_7$, as indicated in the Data I/O Control Table. With $\overline{\mathrm{EAB}}$ LOW, A LOW signal on the A-to-B Latch Enable ($\overline{\mathrm{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\mathrm{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\mathrm{EAB}}$ and $\overline{\mathrm{OEAB}}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{\mathrm{EBA}}$, $\overline{\mathrm{LEBA}}$ and $\overline{\mathrm{OEBA}}$ inputs.

Data I/O Control Table†

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{\mathrm{EAB}}$	$\overline{\mathrm{LEAB}}$	$\overline{\mathrm{OEAB}}$	A-to-B	$B_0 - B_7$
H	X	X	Storing	High Z
X	H	—	Storing	—
X	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

*Before $\overline{\mathrm{LEAB}}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
† A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{\mathrm{EBA}}$, $\overline{\mathrm{LEBA}}$ and $\overline{\mathrm{OEBA}}$

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions
			Min	Typ	Max		
V_{OH}	Output HIGH Voltage $B_0 - B_7$	XM	2.0			V	$I_{OH} = -12$ mA
		XC					$I_{OH} = -15$ mA
V_{OH}	Output HIGH Voltage A_n, B_n		2.4			V	$I_{OH} = -3.0$ mA
V_{OL}	Output LOW Voltage $B_0 - B_7$	XM				V	$I_{OL} = 48$ mA
		XC			0.55		$I_{OL} = 64$ mA
I_{IH}	Input HIGH Current Breakdown Test — A_n, B_n				100	μA	V_{CC} = Max, $V_{IN} = 5.5$ V
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH — A_n, B_n				70	μA	V_{CC} = Max, $V_{OUT} = 2.4$ V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW — A_n, B_n				0.6	mA	V_{CC} = Max, $V_{OUT} = 0.5$ V
I_{OS}	Output Short-circuit Current $B_0 - B_7$		-100		-225	mA	V_{CC} = Max
I_{CC}	Power Supply Current			95	140	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	4.0 4.0	7.0 7.0	10 10					ns	3-1 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n	5.5 5.5	9.0 9.0	12 12					ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n	5.5 5.5	9.0 9.0	12 12					ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	6.0 6.0	10 10	14 14						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	5.0 5.0							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0 2.0								

▨ Test limits in screened columns are preliminary.

54F/74F545

Octal Bidirectional Transceiver

(With 3-State Inputs/Outputs)

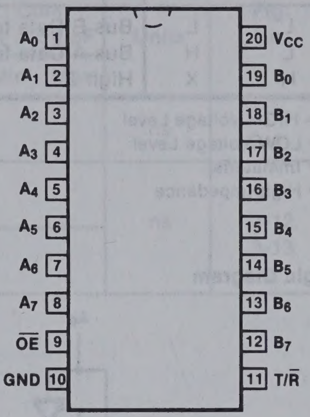
Description

The 'F545 is an 8-bit, 3-state, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 20 mA bus drive capability on the A ports and 64 mA bus drive capability on the B ports.

One input, Transmit/Receive (T/$\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition.

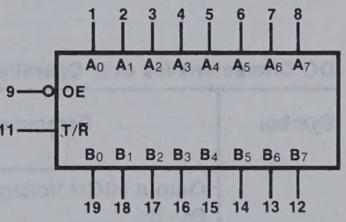
- **Higher Drive than 8304**
- **8-Bit Bidirectional Data Flow Reduces System Package Count**
- **3-State Inputs/Outputs for Interfacing with Bus-oriented Systems**
- **20 mA and 64 mA Bus Drive Capability on A and B Ports, Respectively**
- **Transmit/Receive and Output Enable Simplify Control Logic**
- **Hysteresis on Bus Inputs**

Connection Diagram



A_0 1
A_1 2
A_2 3
A_3 4
A_4 5
A_5 6
A_6 7
A_7 8
$\overline{OE}$ 9
GND 10
20 V_{CC}
19 B_0
18 B_1
17 B_2
16 B_3
15 B_4
14 B_5
13 B_6
12 B_7
11 T/$\overline{R}$

Logic Symbol



1 2 3 4 5 6 7 8
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
9 OE
11 T/R
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F545PC		9Z
Ceramic DIP (D)	74F545DC	54F545DM	4E
Flatpak (F)		54F545FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

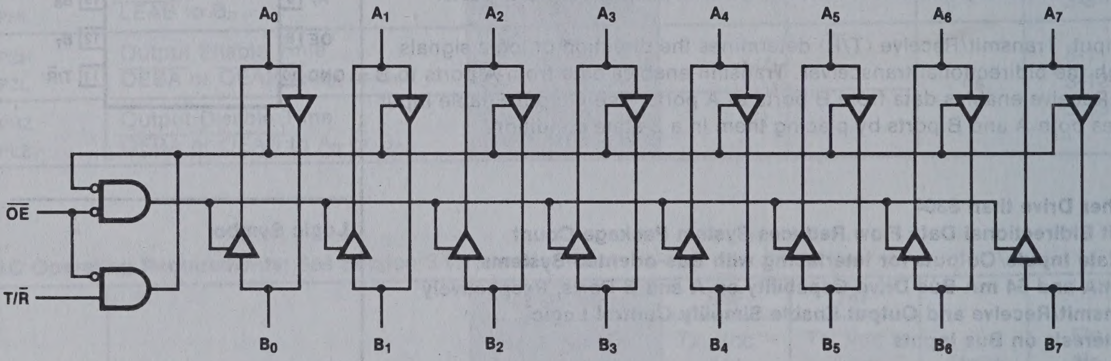
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.875
T/$\overline{R}$	Transmit/Receive Input	0.5/0.625
$A_0 - A_7$	Side A 3-State Inputs or 3-State Outputs	1.75/0.625 25/12.5
$B_0 - B_7$	Side B 3-State Inputs or 3-State Outputs	1.75/0.625 25/40 (30)

Truth Table

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions	
			Min	Typ	Max			
V_{OH}	Output HIGH Voltage $B_0 - B_7$	XM	2.0			V	I_{OH} = −12 mA	V_{CC} = Min
		XC	2.0				I_{OH} = −15 mA	
	Output HIGH Voltage $B_0 - B_7$		2.4			V	I_{OH} = −3.0 mA	
V_{OL}	Output LOW Voltage $B_0 - B_7$	XM			0.55	V	I_{OL} = 48 mA	V_{CC} = Min
		XC			0.55		I_{OL} = 64 mA	
$V_{T+} - V_{T-}$	Hysteresis Voltage $B_0 - B_7$		200	400		mV	V_{CC} = Min	
I_{IH}	Input HIGH Current Breakdown Test — A_n, B_n				100	µA	V_{CC} = Max, V_{IN} = 5.5 V	
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH — A_n, B_n				70	µA	V_{CC} = Max, V_{OUT} = 2.7 V	
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW — A_n, B_n				1.0	mA	V_{CC} = Max, V_{OUT} = 0.5 V	
I_{OS}	Output Short-circuit Current $B_0 - B_7$		-100		-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			128	192	mA	V_{CC} = Max	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	6.5	9.1					ns	3-1
t_{PHL}	A_n to B_n or B_n to A_n	3.5	6.5	9.1						3-4
t_{PZH}	Output Enable Time	4.0	7.0	10					ns	3-1
t_{PZL}		5.5	8.5	14						3-12
t_{PHZ}	Output Disable Time	5.5	8.5	14						3-13
t_{PLZ}		4.0	7.0	10						

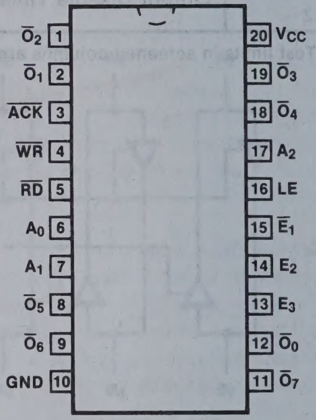
▨ Test limits in screened columns are preliminary.

54F/74F547

Octal Decoder/Demultiplexer

(With Address Latches and Acknowledge)

Connection Diagram


$\overline{O}_2$ 1
$\overline{O}_1$ 2
$\overline{\text{ACK}}$ 3
$\overline{\text{WR}}$ 4
$\overline{\text{RD}}$ 5
A_0 6
A_1 7
$\overline{O}_5$ 8
$\overline{O}_6$ 9
GND 10
20 V_{CC}
19 $\overline{O}_3$
18 $\overline{O}_4$
17 A_2
16 LE
15 $\overline{E}_1$
14 E_2
13 E_3
12 $\overline{O}_0$
11 $\overline{O}_7$

Description

The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple chip selection in a microprocessor system, it contains one active-LOW and two active-HIGH Enables to conserve address space. Also included is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

- **3-to-8 Line Address Decoder**
- **Address Storage Latches**
- **Multiple Enables for Address Extension**
- **Open-collector Acknowledge Output**

Ordering Code: See Section 6

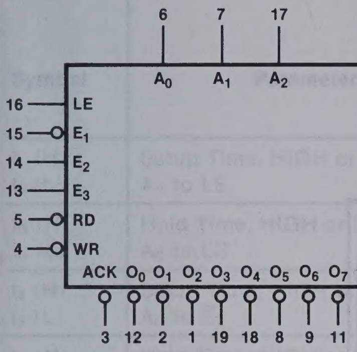
Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F547PC		9Z
Ceramic DIP (D)	74F547DC	54F547DM	4E
Flatpak (F)		54F547FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_2$	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$	Chip Enable Input (Active LOW)	0.5/0.375
E_2, E_3	Chip Enable Inputs	0.5/0.375
LE	Latch Enable Input	0.5/0.375
$\overline{\text{RD}}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{\text{WR}}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{\text{ACK}}$	Open-collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0 - \overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Functional Description

When enabled, the 'F547 accepts the $A_0 - A_2$ Address inputs and decodes them to select one of eight active-LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. With LE HIGH, the Address latches are transparent and the output selection changes each time the $A_0 - A_2$ address changes. When LE is LOW, the latches store the last valid address preceding the HIGH-to-LOW transition of the LE input signal. For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together, such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open-collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when $\overline{E}_1$, E_2 and E_3 are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Decoder Truth Table*

INPUTS			OUTPUTS							
A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

*Assuming $\overline{E}_1$, LOW, E_2 and E_3 HIGH

Latch and Output Status Table

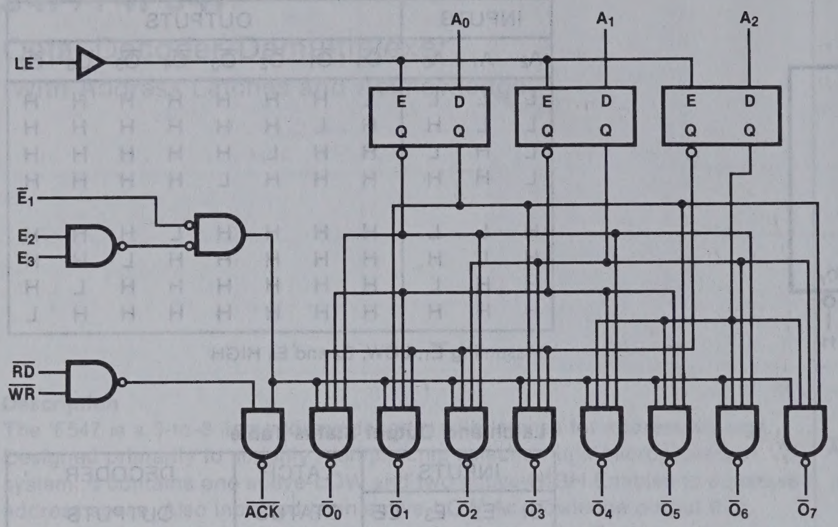
INPUTS				LATCH	DECODER
$\overline{E}_1$	E_2	E_3	LE	STATUS	OUTPUTS
X	X	X	H	Transparent	—
L	H	H	L	Storing	Selected Output LOW
H	X	X	X	Storing	All Outputs HIGH
X	L	X	X	Storing	All Outputs HIGH
X	X	L	X	Storing	All Outputs HIGH

Acknowledge Truth Table

INPUTS					OUTPUT
$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		22	33	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.0 3.0	5.5 5.5	8.0 8.0					ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	3.0 3.0	5.5 5.5	8.0 8.0					ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.0 3.0	5.5 5.5	8.0 8.0					ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{O}_n$	4.0 4.0	6.5 6.5	9.0 9.0					ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	9.0 3.0	11.5 5.5	14 8.0					ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{ACK}$	10 4.0	12.5 6.5	15 9.0					ns	3-1 3-3

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to LE	2.0 2.0							ns	3-15
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to LE	3.0 3.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{E}_1$	2.0 2.0							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{E}_1$	3.0 3.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to E_2, E_3	4.0 4.0							ns	3-15
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to E_2, E_3	3.0 3.0								
t_w (H)	LE Pulse Width HIGH	6.0							ns	3-7

▨ Test limits in screened columns are preliminary.

54F/74F548

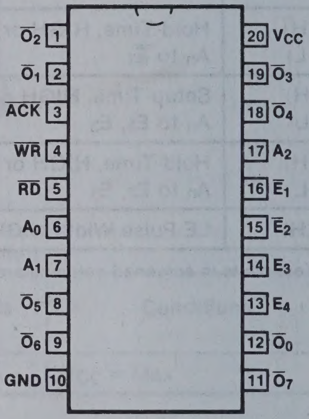
Octal Decoder/Demultiplexer
(With Acknowledge)

Description

The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are active LOW and two are active HIGH for maximum addressing versatility. Also provided is an active-LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

- **3-to-8 Line Address Decoder**
- **Multiple Enables for Address Extension**
- **Open-collector Acknowledge Output**
- **Active-LOW Decoder Outputs**

Connection Diagram



$\overline{O}_2$ 1
$\overline{O}_1$ 2
$\overline{ACK}$ 3
$\overline{WR}$ 4
$\overline{RD}$ 5
A_0 6
A_1 7
$\overline{O}_5$ 8
$\overline{O}_6$ 9
GND 10
20 V_{CC}
19 $\overline{O}_3$
18 $\overline{O}_4$
17 A_2
16 $\overline{E}_1$
15 $\overline{E}_2$
14 E_3
13 E_4
12 $\overline{O}_0$
11 $\overline{O}_7$

Ordering Code: See Section 6

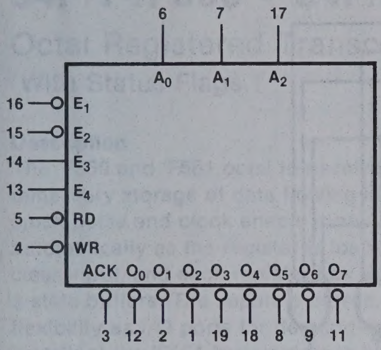
Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F548PC		9Z
Ceramic DIP (D)	74F548DC	54F548DM	4E
Flatpak (F)		54F548FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$A_0 - A_2$	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Chip Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Chip Enable Inputs	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open-collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0 - \overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Functional Description

When enabled, the 'F548 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active-LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. When one or more Enables is inactive, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open-collector Acknowledge ($\overline{\text{ACK}}$) output is normally HIGH (i.e. OFF) and goes LOW when the Enables are all active and either the Read ($\overline{\text{RD}}$) or Write ($\overline{\text{WR}}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

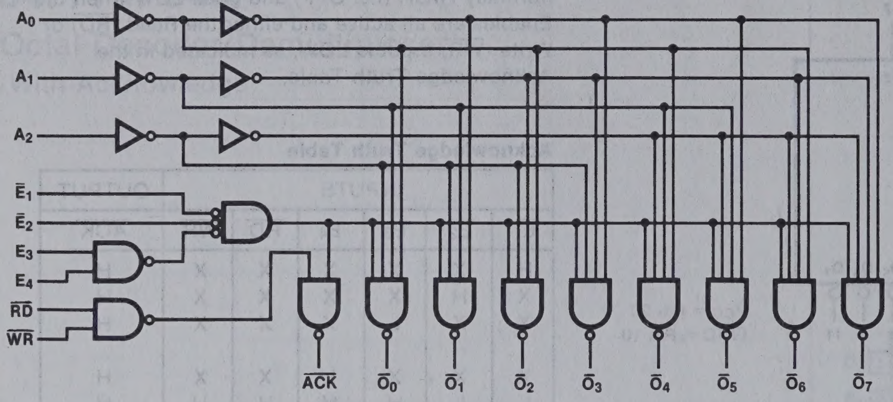
INPUTS						OUTPUT
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{ACK}}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

Decoder Truth Table

INPUTS							OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Logic Diagram


A_0
A_1
A_2
$\overline{E}_1$
$\overline{E}_2$
E_3
E_4
$\overline{RD}$
$\overline{WR}$
$\overline{ACK}$
$\overline{O}_0$
$\overline{O}_1$
$\overline{O}_2$
$\overline{O}_3$
$\overline{O}_4$
$\overline{O}_5$
$\overline{O}_6$
$\overline{O}_7$

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		18	27	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.0	5.5	8.0					ns	3-1
t_{PHL}		3.0	5.5	8.0						3-10
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0	5.5	8.0					ns	3-1
t_{PHL}		3.0	5.5	8.0						3-4
t_{PLH}	Propagation Delay E_3 or E_4 to $\overline{O}_n$	4.0	6.5	9.0					ns	3-1
t_{PHL}		4.0	6.5	9.0						3-3
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{ACK}$	9.0	11.5	14					ns	3-1
t_{PHL}		3.0	5.5	8.0						3-4
t_{PLH}	Propagation Delay E_3 or E_4 to $\overline{ACK}$	10	12.5	15					ns	3-1
t_{PHL}		4.0	6.5	9.0						3-3
t_{PLH}	Propagation Delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	9.0	11.5	14					ns	3-1
t_{PHL}		3.0	5.5	8.0						3-4

▨ Test limits in screened columns are preliminary.

54F/74F550 • 54F/74F551

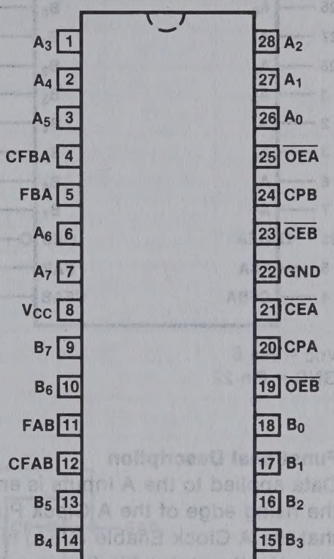
Octal Registered Transceiver
(With Status Flags)

Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its 3-state buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

- **8-Bit Bidirectional I/O Port with Handshake**
- **Back-to-Back Registers for Storage**
- **Register Status Flag Flip-Flops**
- **Separate Edge-detecting Clears for Flags**
- **Inverting and Non-Inverting Versions**
- **A Outputs Sink 20 mA, B Outputs Sink 64 mA**

Connection Diagram
('F550 shown*)



*'F551 has inverting outputs

Ordering Code: See Section 6

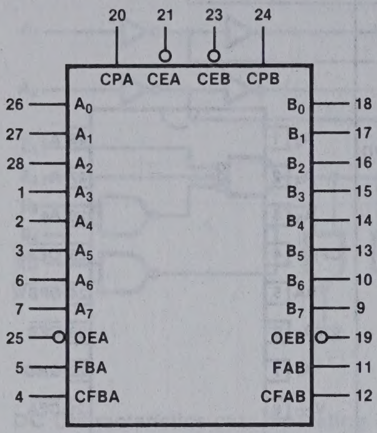
Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F550PC, 74F551PC		9Y
Ceramic DIP (D)	74F550DC, 74F551DC	54F550DM, 54F551DM	8S
Flatpak (F)		54F550FM, 54F551FM	2E

Input Loading/Fan-Out: See Section 3 for U.L. definitions

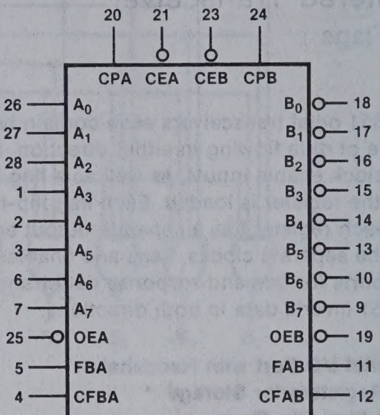
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	0.5/0.375
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{CEA}$	A-to-B Clock Enable Input (Active LOW)	0.5/0.375
$\overline{CEB}$	B-to-A Clock Enable Input (Active LOW)	0.5/0.375
$\overline{OEA}$	A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEB}$	B Output Enable Input (Active LOW)	0.5/0.375
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	0.5/0.5
CFBA	B-to-A Flag Clear Input (Active Rising Edge	0.5/0.5
$A_0 - A_7$	A-to-B Data Inputs or 3-State B-to-A Outputs	1.75/0.375 25/12.5
$B_0 - B_7$	B-to-A Data Inputs or 3-State A-to-B Outputs	1.75/0.375 25/40 (30)
FAB	A-to-B Status Flag Output (Active HIGH)	0.5/0.375
FBA	B-to-A Status Flag Output (Active HIGH)	0.5/0.375

Logic Symbols

'F550


20
21
23
24
CPA
CEA
CEB
CPB
26
27
28
1
2
3
6
7
25
5
4
A0
A1
A2
A3
A4
A5
A6
A7
OEA
FBA
CFBA
B0
B1
B2
B3
B4
B5
B6
B7
OEB
FAB
CFAB
18
17
16
15
14
13
10
9
19
11
12

'F551


20
21
23
24
CPA
CEA
CEB
CPB
26
27
28
1
2
3
6
7
25
5
4
A0
A1
A2
A3
A4
A5
A6
A7
OEA
FBA
CFBA
B0
B1
B2
B3
B4
B5
B6
B7
OEB
FAB
CFAB
18
17
16
15
14
13
10
9
19
11
12

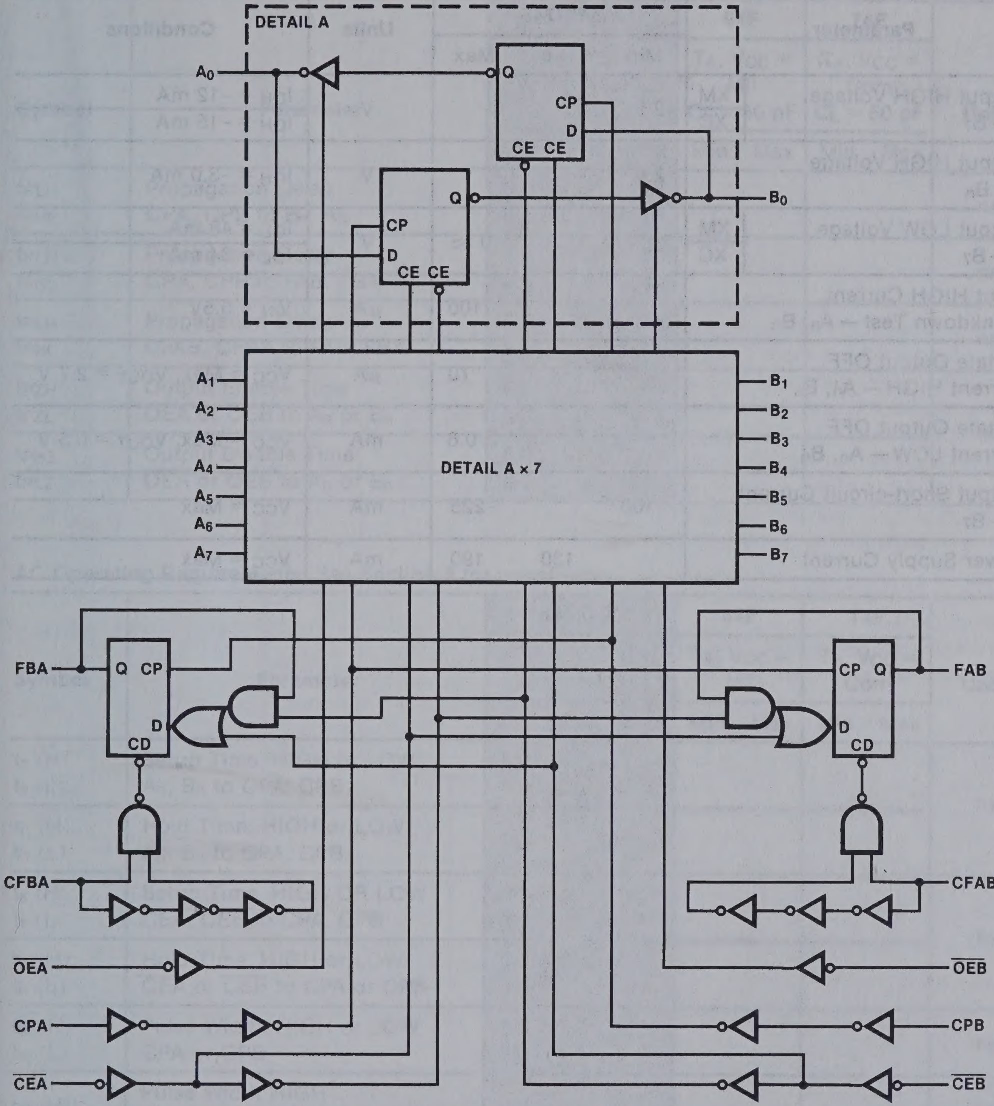
V_{CC} = Pin 8
GND = Pin 22

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{\text{CEA}}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{\text{OEB}}$) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH transition to the CFAB input. Optionally, the $\overline{\text{OEA}}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{\text{CEB}}$ and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on $\overline{\text{OEA}}$ enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

Logic Diagram ('F550 shown)


DETAIL A
A0
Q
CP
D
CE CE
Q
CP
D
CE CE
B0
A1
A2
A3
A4
A5
A6
A7
DETAIL A × 7
B1
B2
B3
B4
B5
B6
B7
FBA
Q CP
D
CD
CP Q
D
CD
FAB
CFBA
CFAB
OEA
OEB
CPA
CPB
CEA
CEB

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions
			Min	Typ	Max		
V_{OH}	Output HIGH Voltage $B_0 - B_7$	XM	2.0			V	$I_{OH} = -12$ mA
		XC					$I_{OH} = -15$ mA
V_{OH}	Output HIGH Voltage A_n, B_n		2.4			V	$I_{OH} = -3.0$ mA
V_{OL}	Output LOW Voltage $B_0 - B_7$	XM			0.55	V	$I_{OL} = 48$ mA
		XC					$I_{OL} = 64$ mA
I_{IH}	Input HIGH Current Breakdown Test — A_n, B_n				100	µA	$V_{IN} = 5.5V$
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH — A_n, B_n				70	µA	V_{CC} = Max, $V_{OUT} = 2.7$ V
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW — A_n, B_n				0.6	mA	V_{CC} = Max, $V_{OUT} = 0.5$ V
I_{OS}	Output Short-circuit Current $B_0 - B_7$		-100		-225	mA	V_{CC} = Max
I_{CC}	Power Supply Current			130	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	6.5 6.5	11 11	15.5 15.5					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to FAB, FBA	4.0 4.0	7.0 7.0	10 10					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CFAB, CFBA to FAB, FBA	5.5 5.5	9.0 9.0	12.5 12.5					ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	6.0 6.0	10 10	14 14					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	6.0 6.0	10 10	14 14						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	5.0 5.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	0 0								
t_s (H) t_s (L)	Setup Time, HIGH OR LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	8.0 8.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	0 0								
t_w (H) t_w (L)	Pulse Width, HIGH or LOW CPA or CPB	8.0 8.0							ns	3-7
t_w (H)	Pulse Width HIGH CFAB or CFBA	8.0							ns	3-11
t_{rec}	Recovery Time CFAB, CFBA to CPA, CPB	15							ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F557 • 54F/74F558

8-Bit By 8-Bit Multipliers

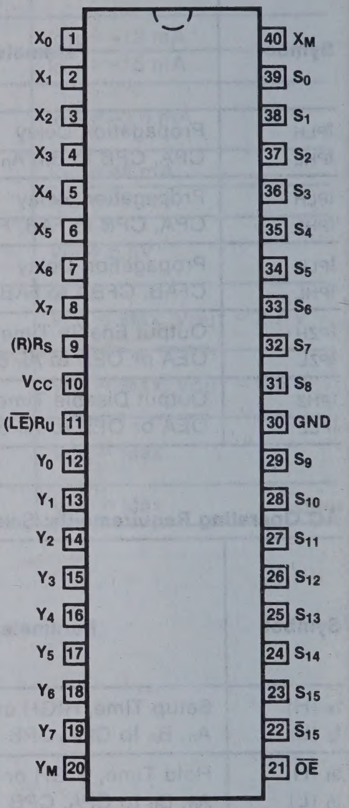
(With 3-State Outputs)

Description

The ’F557 and ’F558 are high-speed combinatorial arrays that multiply two 8-bit unsigned or signed twos complement numbers and provide the 16-bit unsigned or signed product. Each input operand X and Y has a mode control input that determines whether the number is treated as signed or unsigned. Additional inputs, R_S and R_U for the ’F558 or R for the ’F557, allow the addition of a bit for rounding to the best signed or unsigned fractional 8-bit result. For expansion during signed or mixed multiplication, both the true and complement outputs of the most significant bit are available. The ’F557 has output latches that store the results when $\overline{LE}$ is HIGH. Both devices have 3-state outputs for bus applications.

- **Unsigned, Signed or Mixed Multiplication**
- **Full 16-Bit Product Outputs**
- **MSB Complement Output for Signed Expansion**
- **Rounding Inputs for Fractional 8-Bit Product**

Connection Diagram


X_0 1
X_1 2
X_2 3
X_3 4
X_4 5
X_5 6
X_6 7
X_7 8
(R)R_S 9
V_{CC} 10
($\overline{LE}$)R_U 11
Y_0 12
Y_1 13
Y_2 14
Y_3 15
Y_4 16
Y_5 17
Y_6 18
Y_7 19
Y_M 20
21 $\overline{OE}$
22 $\overline{S}_{15}$
23 S_{15}
24 S_{14}
25 S_{13}
26 S_{12}
27 S_{11}
28 S_{10}
29 S_9
30 GND
31 S_8
32 S_7
33 S_6
34 S_5
35 S_4
36 S_3
37 S_2
38 S_1
39 S_0
40 X_M

Pin assignments shown are for ’F558. $\overline{LE}$ and R shown in parentheses are pin assignments for ’F557.

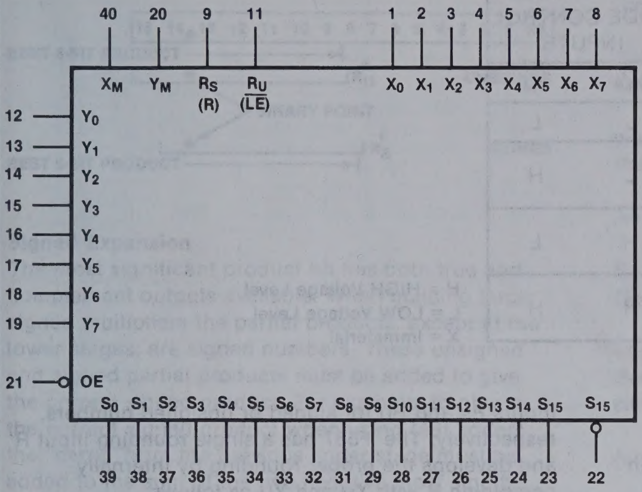
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F557PC, 74F558PC		9L
Ceramic DIP (D)	74F557DC, 74F558DC	54F557DM, 54F558DM	4W

Input Loading/Fan-Out: See Section 3 for U.L. definitions

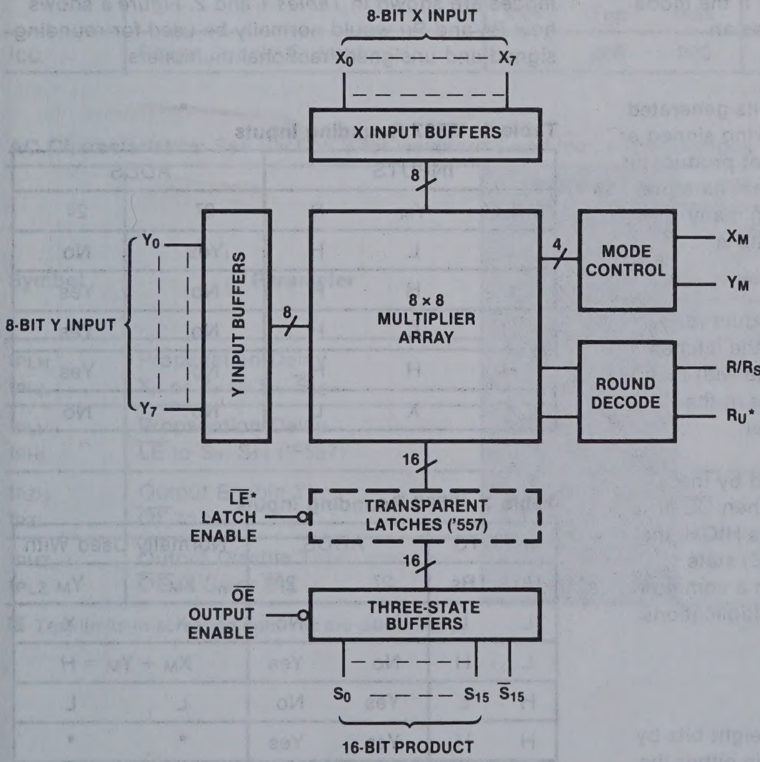
Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$X_0 - X_7$	Multiplicand Inputs	0.5/0.5
$Y_0 - Y_7$	Multiplier Inputs	0.5/0.5
X_M	Multiplicand Sign Control Input	0.5/0.5
Y_M	Multiplier Sign Control Input	0.5/0.5
R	Rounding Input (’F557)	0.5/0.5
R_S	Signed Number Rounding Input (’F558)	0.5/0.5
R_U	Unsigned Number Rounding Input (’F558)	0.5/0.5
$\overline{LE}$	Latch Enable Input (Active LOW) (’F557)	0.5/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.5
$S_0 - S_{15}$	Product Outputs	50/12.5
$\overline{S}_{15}$	MSB Complement Output	50/12.5

Logic Symbol


40
20
9
11
1
2
3
4
5
6
7
8
X_M
Y_M
R_S (R)
R_U ($\overline{LE}$)
X_0 X_1 X_2 X_3 X_4 X_5 X_6 X_7
12 Y_0
13 Y_1
14 Y_2
15 Y_3
16 Y_4
17 Y_5
18 Y_6
19 Y_7
21 OE
S_0 S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10} S_{11} S_{12} S_{13} S_{14} S_{15} $\overline{S_{15}}$
39 38 37 36 35 34 33 32 31 29 28 27 26 25 24 23 22

V_{CC} = Pin 10
GND = Pin 30

Logic Diagram


8-BIT X INPUT
X_0
X_7
X INPUT BUFFERS
8
Y_0
8-BIT Y INPUT
Y_7
Y INPUT BUFFERS
8
8 × 8 MULTIPLIER ARRAY
4
MODE CONTROL
X_M
Y_M
ROUND DECODE
R/R_S
R_U*
16
$\overline{LE}$* LATCH ENABLE
TRANSPARENT LATCHES ('557)
16
$\overline{OE}$ OUTPUT ENABLE
THREE-STATE BUFFERS
S_0
S_{15}
$\overline{S_{15}}$
16-BIT PRODUCT

*Pin 11 is $\overline{LE}$ for 'F557 and R_U for 'F558.

Mode Select Table

OPERATING MODE	INPUT DATA		MODE CONTROL INPUTS	
	X_0-X_7	Y_0-Y_7	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos Complement	L	H
	Twos Complement	Unsigned	H	L
Signed	Twos Complement	Twos Complement	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

The 'F557 and 'F558 multipliers are 8 x 8 combinatorial logic arrays capable of multiplying numbers in unsigned, signed twos complement or mixed notation. Each 8-bit input operand X and Y has an associated mode control which determines whether the array treats the number as signed or unsigned. If the mode control X_M or Y_M is HIGH, the operand is treated as a twos complement number with the most significant bit having a negative weight; if the mode control is LOW, the operand is treated as an unsigned number.

The multipliers provide all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication, the most significant product bit has both true and complement available. Therefore, an adder may be used as a subtractor in many applications and the need for SSI circuits is eliminated.

The 'F557 has latches that store the product for pipelined operations. When $\overline{LE}$ is LOW the latches are transparent and their outputs change with their inputs. When $\overline{LE}$ is HIGH the latches are in the storage mode and new data cannot enter.

The 3-state output buffers are controlled by the active-LOW Output Enable $\overline{OE}$ input. When $\overline{OE}$ is LOW, the outputs are active; when $\overline{OE}$ is HIGH, the outputs are in a high impedance (high-Z) state. Several multipliers can be connected on a common bus or used in a pipeline system for multiplications in higher speed systems.

Rounding

The 16-bit product can be truncated to eight bits by using the rounding input(s) to add one in either the 2^7 adder for unsigned numbers or in the 2^6 adder for signed numbers. The 'F558 has separate rounding inputs R_S and R_U for signed or unsigned numbers, respectively. The 'F557 has a single rounding input R and develops the proper rounding by internally combining R with X_M and Y_M as follows:

$R_U = \overline{X_M} \cdot \overline{Y_M} \cdot R$ = unsigned rounding input to 2^7 adder
$R_S = (X_M \pm Y_M)R$ = signed rounding input to 2^6 adder

Rounding input levels and results for the various modes are shown in *Tables 1* and *2*. *Figure a* shows how R_S and R_U would normally be used for rounding signed and unsigned fractional multipliers.

Table 1 'F557 Rounding Inputs

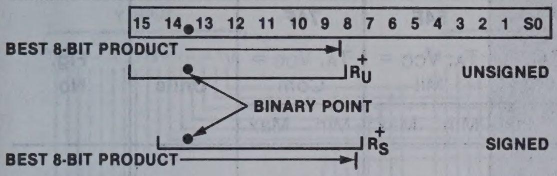
INPUTS			ADDS	
X_M	Y_M	R	2^7	2^6
L	L	H	Yes	No
L	H	H	No	Yes
H	L	H	No	Yes
H	H	H	No	Yes
X	X	L	No	No

Table 2 'F558 Rounding Inputs

INPUTS		ADDS		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	No	No	X	X
L	H	No	Yes	$X_M + Y_M = H$	
H	L	Yes	No	L	L
H	H	Yes	Yes	*	*

* Most rounding applications require a HIGH level for R_U or R_S, but not both.

Fig. a Rounded Products



Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products, except at the lower stages, are signed numbers. These unsigned and signed partial products must be added to give the correct signed product. For example, to obtain the correct signed product when using MSI adders the "carry" from the previous adder stage must be added to the sum of the two negative most significant partial product bits. The result of this addition must be a positive sum and a negative carry (borrow). The equations are:

$$S = A + B + C$$
$$C_O = A \cdot B + B \cdot \overline{C} + \overline{C} \cdot A$$

where C is the Carry In and A and B the sign bits of the two partial products.

An adder produces the equations:

$$S = A + B + C$$
$$C_O = A \cdot B + B \cdot C + C \cdot A$$

Therefore, if the inversion of A and B is used, then the adder produces the inversion of the negative carry since

$$A \cdot B + B \cdot \overline{C} + \overline{C} \cdot A = \overline{A} \cdot \overline{B} + \overline{B} \cdot C + \overline{A} \cdot C$$

and the sum remains the same.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		200	280	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay		45	70					ns	3-1
t_{PHL}	X_n or Y_n to S_n, $\overline{S}_{15}$		45	70						3-10
t_{PLH}	Propagation Delay	20							ns	3-1
t_{PHL}	$\overline{LE}$ to S_n, $\overline{S}_{15}$ ('F557)	20								3-8
t_{PZH}	Output Enable Time	6.0	10	14					ns	3-1 3-12 3-13
t_{PZL}	$\overline{OE}$ to S_n or $\overline{S}_{15}$	6.0	10	14						
t_{PHZ}	Output Disable Time	9.0	15	21						
t_{PLZ}	$\overline{OE}$ to S_n or $\overline{S}_{15}$	6.0	10	14						

▨ Test limits in screened columns are preliminary.

AC Operating Requirements ('F557 Only): See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW, X_n or Y_n to $\overline{LE}$	65 65							ns	3-14
t_h (H) t_h (L)	Hold Time, HIGH or LOW, X_n or Y_n to $\overline{LE}$	0 0								
t_w (L)	$\overline{LE}$ Pulse Width LOW	10							ns	3-8

▨ Test limits in screened columns are preliminary.

Applications

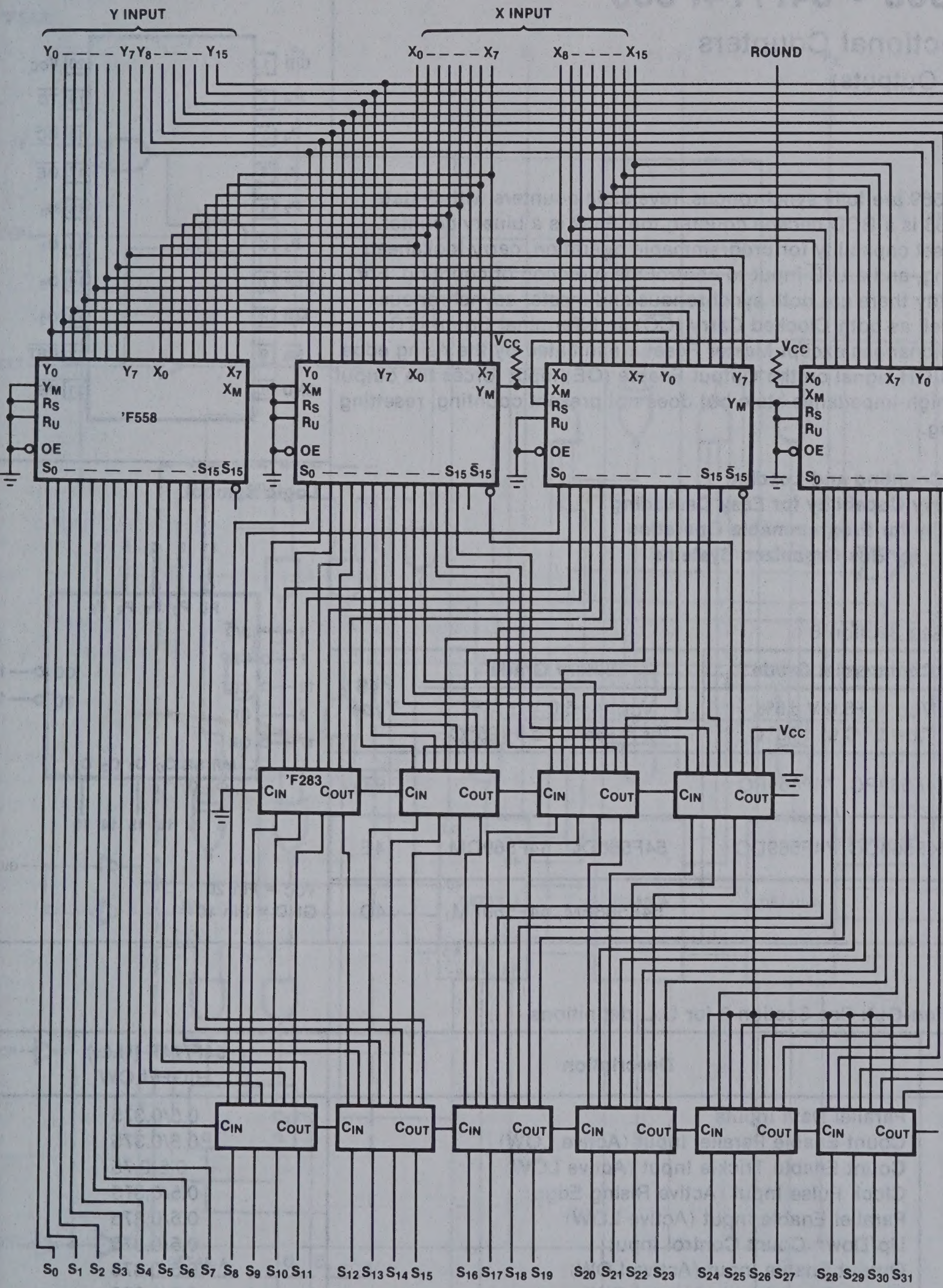
16 x 16 Twos Complement Multiplier

The 'F558 8 x 8 multiplier can be used with standard MSI adder circuits to build larger multipliers. *Figure b* illustrates the use of four 'F558 multipliers and ten 16-pin 4-bit 54F/74F283 adders to form a 16 x 16-bit twos complement multiplier with a typical multiplication time of 90 ns. The 16-bit operands are split up into 8-bit sections:

$$X \cdot Y = (X_{0-7} + X_{8-15}2^8) \cdot (Y_{0-7} + Y_{8-15}2^8)$$
$$= X_{0-7} \cdot Y_{0-7} + 2^8\,(X_{0-7} \cdot Y_{8-15} + X_{8-15} \cdot Y_{0-7}) =$$
$$+2^{16}\,(X_{8-15} \cdot Y_{8-15})$$

Since $X_8 - X_{15}$ and $Y_8 - Y_{15}$ are signed numbers, the most significant bit of all the partial products (except the first) carries a negative weight. Therefore, at these negative bit positions the partial product bits must be subtracted rather than added. This subtraction is done in the middle of the network at the 2^{15} bit position by using the inverted output of the most significant product bits from the multipliers to obtain a 'borrow' signal from the last sum output of the appropriate 'F283. This 'borrow' is then used to either add zero or minus 1 to the remaining 8-bit adder section. The mode control inputs of the four 'F558 devices are tied to the logic levels required to produce the correctly signed partial products. Rounding to the best 16-bit fractional product is made by tying the R_S input of one of the middle multipliers to V_{CC}. Appropriate connection of the adders and mode control logic levels will yield 16 x 16 unsigned multiplication.

Fig. b High-speed 16 x 16 Twos Complement Multiplication


Y INPUT
X INPUT
Y0 – – – – Y7 Y8 – – – – Y15
X0 – – – – X7
X8 – – – – X15
ROUND
VCC
Y0
YM
RS
RU
OE
S0
Y7
X0
X7
XM
'F558
S15 S̄15
Y0
XM
RS
RU
OE
S0
Y7
X0
X7
YM
S15 S̄15
X0
XM
RS
RU
OE
S0
X7
Y0
Y7
YM
S15 S̄15
X0
XM
RS
RU
OE
S0
X7
Y0
Y7
YM
VCC
S15 S̄15
'F283
CIN
COUT
VCC
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11
S12 S13 S14 S15
S16 S17 S18 S19
S20 S21 S22 S23
S24 S25 S26 S27
S28 S29 S30 S31

54F/74F568 • 54F/74F569

4-Bit Bidirectional Counters

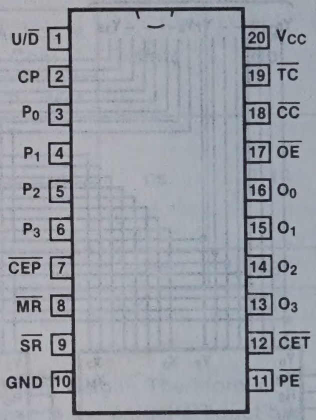
(With 3-State Outputs)

Description

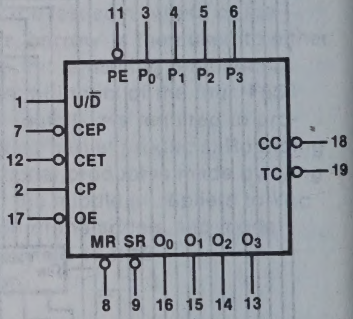
The 'F568 and 'F569 are fully synchronous, reversible counters with 3-state outputs. The 'F568 is a BCD decade counter; the 'F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a $U/\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-impedance state but does not prevent counting, resetting or parallel loading.

- **Synchronous Counting and Loading**
- **Lookahead Carry Capability for Easy Cascading**
- **Preset Capability for Programmable Operation**
- **3-State Outputs for Bus Organized Systems**

Connection Diagram



Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Ordering Code: See Section 6

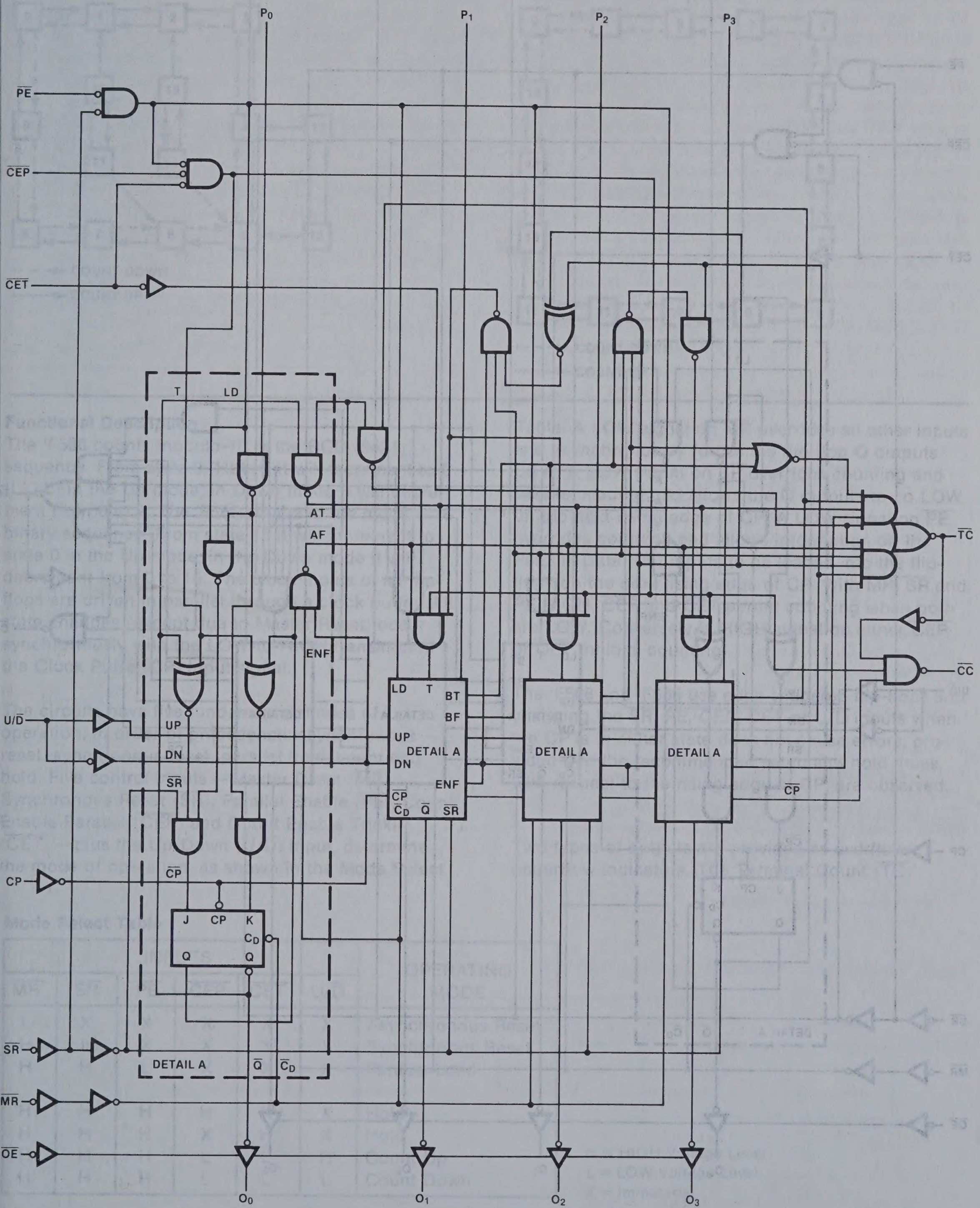
Pkgs	**Commercial Grade**	**Military Grade**	**Pkg Type**
	$V_{CC} = +5.0$ V ±5%, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0$ V ±10%, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F568PC, 74F569PC		9Z
Ceramic DIP (D)	74F568DC, 74F569DC	54F568DM, 54F569DM	4E
Flatpak (F)		54F568FM, 54F569FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	**Description**	**54F/74F (U.L.) HIGH/LOW**
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
$U/\overline{D}$	Up/Down Count Control Input	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
$O_0 - O_3$	3-State Parallel Data Outputs	25/12.5
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5
$\overline{CC}$	Clocked Carry Output (Active LOW)	25/12.5

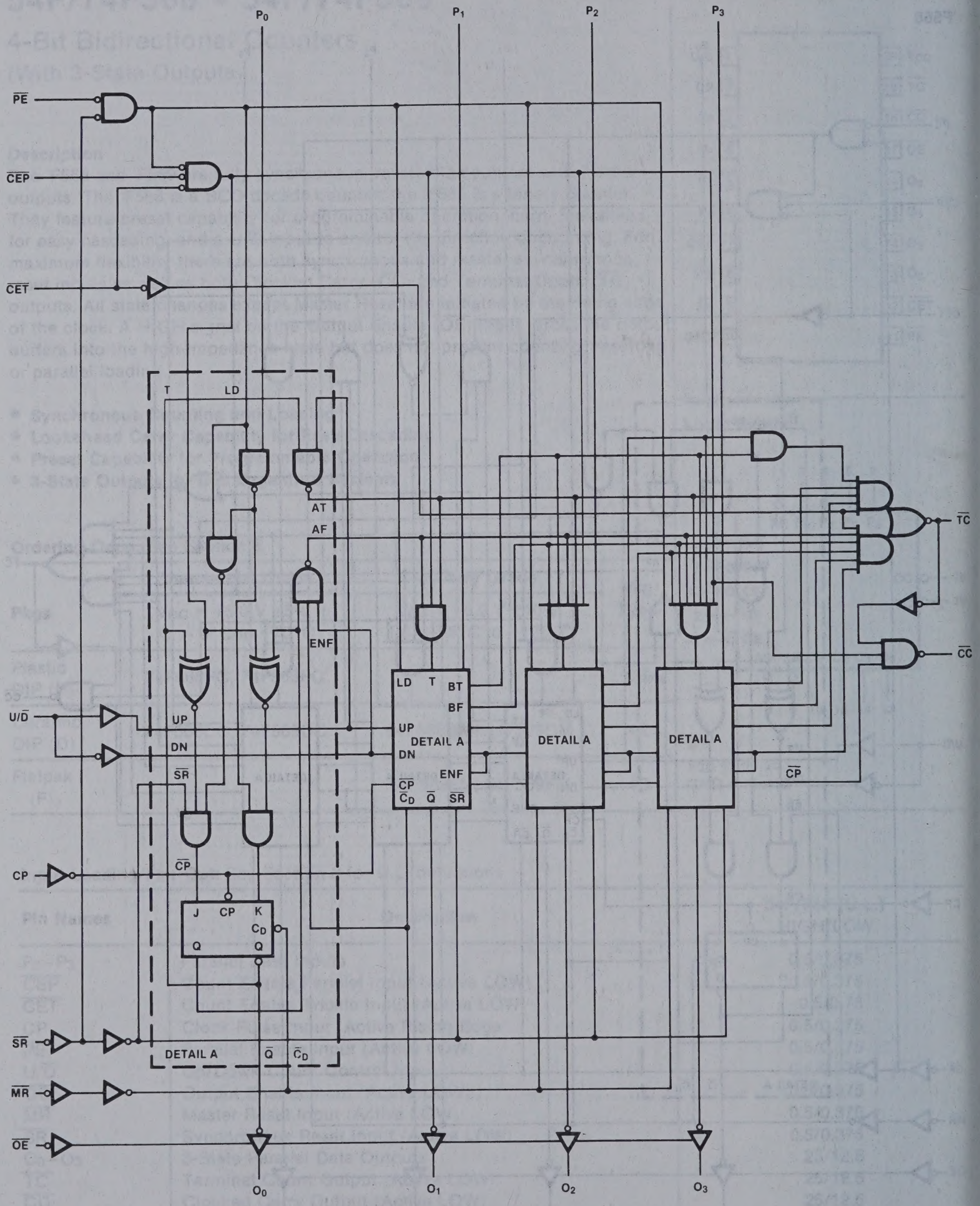
Logic Diagrams

'F568


P_0
P_1
P_2
P_3
$\overline{PE}$
$\overline{CEP}$
$\overline{CET}$
T
LD
AT
AF
ENF
U/$\overline{D}$
UP
DN
$\overline{SR}$
$\overline{CP}$
J
CP
K
C_D
Q
Q
DETAIL A
$\overline{Q}$
$\overline{C_D}$
LD
T
BT
BF
UP
DETAIL A
DN
ENF
$\overline{CP}$
$\overline{C_D}$
$\overline{Q}$
$\overline{SR}$
DETAIL A
DETAIL A
$\overline{CP}$
$\overline{TC}$
$\overline{CC}$
$\overline{SR}$
$\overline{MR}$
$\overline{OE}$
O_0
O_1
O_2
O_3

4

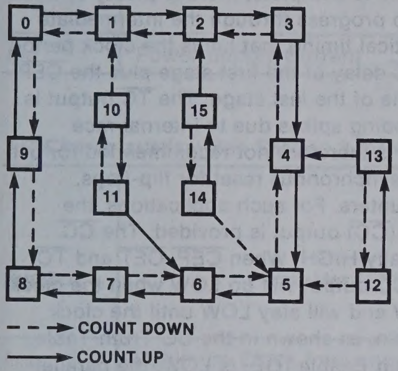
'F569


P$_0$
P$_1$
P$_2$
P$_3$
$\overline{PE}$
$\overline{CEP}$
$\overline{CET}$
U/$\overline{D}$
CP
$\overline{SR}$
$\overline{MR}$
$\overline{OE}$
T
LD
AT
AF
ENF
UP
DN
$\overline{SR}$
$\overline{CP}$
J
CP
K
C$_D$
Q
Q
DETAIL A
$\overline{Q}$
$\overline{C}_D$
LD
T
BT
BF
UP
DETAIL A
DN
ENF
$\overline{CP}$
$\overline{C}_D$
$\overline{Q}$
$\overline{SR}$
DETAIL A
DETAIL A
$\overline{CP}$
$\overline{TC}$
$\overline{CC}$
O$_0$
O$_1$
O$_2$
O$_3$

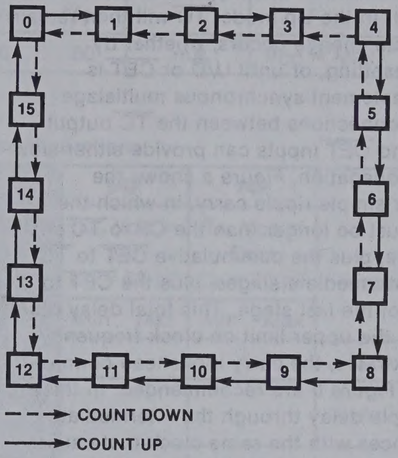
"

State Diagrams

'F568



'F569



Functional Description

The 'F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$) — plus the Up/Down ($U/\overline{D}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'F568 and 'F569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or $U/\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$)

Mode Select Table

INPUTS						OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'F568, 15 for the 'F569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. *Figure a* shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cummulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure b* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$ and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs $O_0 - O_3$ are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces $O_0 - O_3$ to the high-Z state but does not prevent counting, loading or resetting.

$\overline{CC}$ Truth Table

INPUTS				OUTPUT
$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
L	L	L	⊔	⊔

* = $\overline{TC}$ is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Equations:

$$\text{Count Enable} = \overline{CEP} \bullet \overline{CET} \bullet PE$$
$$\text{Up ('F568): } \overline{TC} = Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3 \bullet (\text{Up}) \bullet \overline{CET}$$
$$\text{('F569): } \overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (\text{Up}) \bullet \overline{CET}$$
$$\text{Down (Both): } \overline{TC} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet (\text{Down}) \bullet \overline{CET}$$

Fig a Multistage Counter with Ripple Carry

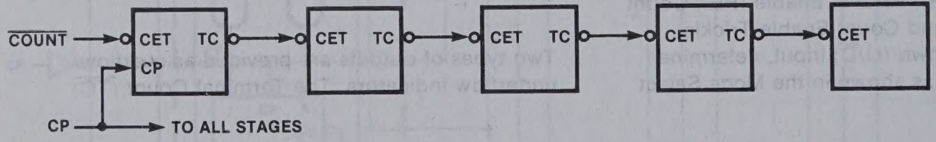
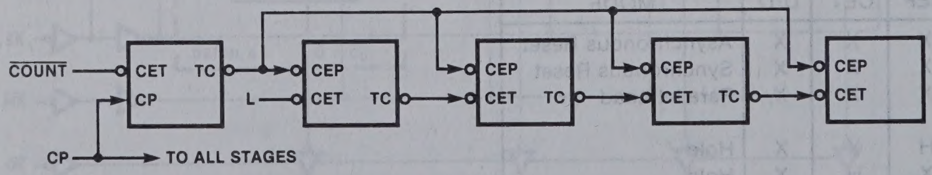


Fig b Multistage Counter with Lookahead Carry



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current		40	60	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25° C, V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Maximum Clock frequency	75							MHz	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	4.0 5.5	7.0 9.0	10 12.5					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	6.5 6.5	10.5 10.5	15 15					ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	4.0 3.5	6.5 5.5	9.0 8.0					ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	4.0 4.5	6.5 7.5	9.0 10					ns	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CC}$	3.5 3.0	6.0 5.0	8.5 7.0					ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$	3.5 4.5	6.0 8.0	8.5 12					ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	6.0	10	14					ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	6.0 7.0	10 12	14 17					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.5 3.5	6.0 6.0	8.5 8.5						

▨ Test limits in screened columns are preliminary.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	5.0 7.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	3.0 3.0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	10 10							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ to CP	10 7.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	14 14							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{SR}$ to CP	8.0 6.0							ns	3-5
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.0 3.0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	4.5 6.5							ns	3-7
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0							ns	3-11
t_{rec}	$\overline{MR}$ Recovery Time	7.0							ns	3-11
t_{rec}	$\overline{SR}$ Recovery Time	8.0							ns	3-11

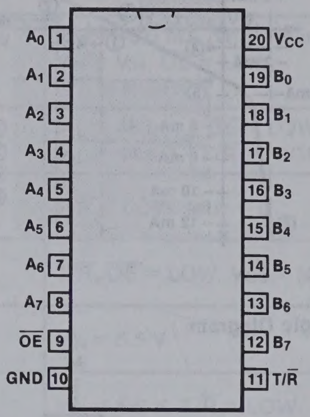
▨ Test limits in screened columns are preliminary.

54F/74F588

Octal Bidirectional Transceiver

(With 3-State Inputs/Outputs and IEEE-488 Termination Resistors)

Connection Diagram



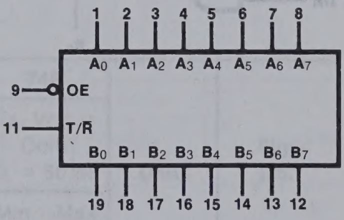
A_0 1
A_1 2
A_2 3
A_3 4
A_4 5
A_5 6
A_6 7
A_7 8
$\overline{OE}$ 9
GND 10
20 V_{CC}
19 B_0
18 B_1
17 B_2
16 B_3
15 B_4
14 B_5
13 B_6
12 B_7
11 $T/\overline{R}$

Description

The 'F588 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20 mA at the A ports and 48 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-impedance condition.

- **Non-inverting Buffers**
- **Bidirectional Data Path**
- **B Outputs Sink 48 mA, Source 15 mA**

Logic Symbol



1 2 3 4 5 6 7 8
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
9 OE
11 T/R
B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7
19 18 17 16 15 14 13 12

V_{CC} = Pin 20
GND = Pin 10

Ordering Code: See Section 6

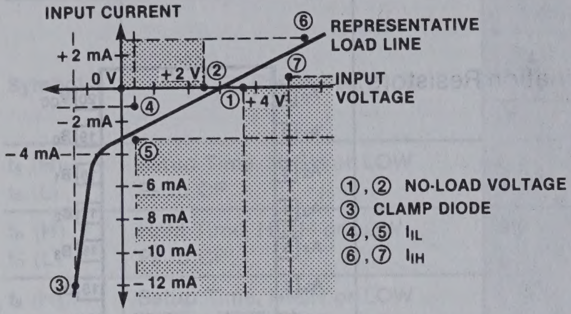
Pkgs	Commercial Grade	Military Grade	Pkg Type
	$V_{CC} = +5.0$ V ±5%, $T_A = 0°C$ to $+70°C$	$V_{CC} = +5.0$ V ±10%, $T_A = -55°C$ to $+125°C$	
Plastic DIP (P)	74F588PC		9Z
Ceramic DIP (D)	74F588DC	54F588DM	4E
Flatpak (F)		54F588FM	4D

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/0.94
$T/\overline{R}$	Transmit/Receive Control Input	0.5/0.47
$A_0 - A_7$	A Port Inputs or	1.75/0.41
	3-State Outputs	75/12.5
$B_0 - B_7$	B Port Inputs or	T*/2.0
	3-State Outputs	130/30

*T = Restive Termination per IEEE-488 Standard

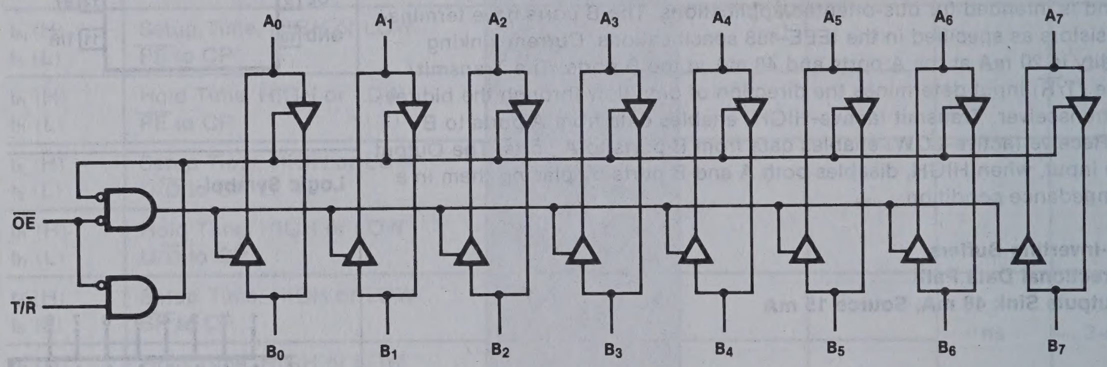
B Port Input Characteristic with T/R̄ LOW



Truth Table

INPUTS		OUTPUTS
O̅E̅	T/R̄	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Impedance

Logic Diagram


A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
O̅E̅
T/R̄
B_0
B_1
B_2
B_3
B_4
B_5
B_6
B_7

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions	
			Min	Typ	Max			
V_{OH}	Output HIGH Voltage A_0-A_7, B_0-B_7		2.4			V	I_{OH} = −3.0 mA, V_{CC} = Min $V_{IN} = V_{IH}$, $\overline{OE}$ = LOW, T/$\overline{R}$ = HIGH	
V_{OL}	Output LOW Voltage B_0-B_7	XM XC			0.55	V	I_{OL} = 48 mA I_{OL} = 64 mA	$\overline{OE}$ = LOW, T/$\overline{R}$ = HIGH
V_{NL}	No-load Voltage B_0-B_7		2.5		3.7	V	T/$\overline{R}$ = LOW, I_{OUT} = 0	
$V_{T+}-V_{T-}$	Hysteresis Voltage B_0-B_7		0.2			V	T/$\overline{R}$, $\overline{OE}$ = LOW, V_{CC} = Min	
I_{IH}	Input HIGH Current Breakdown Test, A_0-A_7				100	µA	V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current B_0-B_7		0.7		2.5	mA	V_{IN} = 5.0 V, T/$\overline{R}$ = LOW	
I_{IL}	Input LOW Current B_0-B_7		1.3		3.2	mA	V_{IN} = 0.4 V, T/$\overline{R}$ = LOW	
$I_{IH}+I_{OZH}$	3-State Output OFF Current HIGH, A_0-A_7				70	µA	V_{IN} = 2.7 V, T/$\overline{R}$ = HIGH V_{CC} = Max	
I_{CC}	Power Supply Current			128	192	mA	$\overline{OE}$ = HIGH, V_{CC} = Max	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	6.5	9.1					ns	3-1
t_{PHL}	A to B or B to A	3.5	6.5	9.1						3-4
t_{PZH}	Output Enable Time	4.0	7.0	10					ns	3-1 3-12 3-13
t_{PZL}	T/$\overline{R}$ or $\overline{OE}$ to A or B	5.5	8.5	14						
t_{PHZ}	Output Disable Time	5.5	8.5	14						
t_{PLZ}	T/$\overline{R}$ or $\overline{OE}$ to A or B	4.0	7.0	10						

▨ Test limits in screened columns are preliminary.

54F/74F673

16-Bit Shift Register

(Serial-in/Serial-Parallel Out)

Description

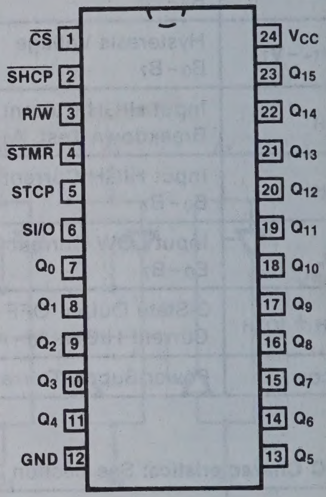
The 'F673 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-state serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via $\overline{STMR}$.

- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-out Storage Register**
- **Recirculating Serial Shifting**
- **Recirculating Parallel Transfer**
- **Common Serial Data I/O Pin**

Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F673PC		9N
Ceramic DIP (D)	74F673DC	54F673DM	6N
Flatpak (F)		54F673FM	4M

Connection Diagram



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
$\overline{STMR}$	Store Master Reset Input (Active LOW)	0.5/0.375
STCP	Store Clock Pulse Input	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SI/O	Serial Data Input or 3-State Serial Output	1.75/0.375 25/12.5
$Q_0 - Q_{15}$	Parallel Data Outputs	25/12.5

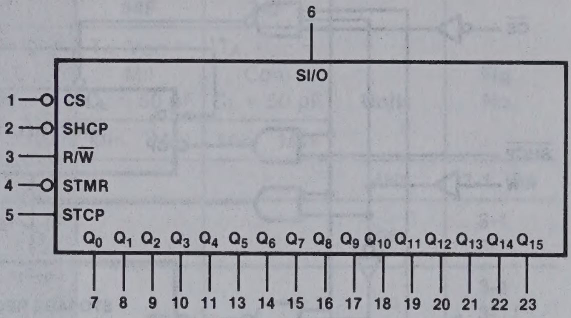
Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high-impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset ($\overline{STMR}$) input that overrides all other inputs and forces the $Q_0 - Q_{15}$ outputs LOW. The storage register is in the Hold mode when either $\overline{CS}$ or the Read/Write (R/$\overline{W}$) input is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

Storage Register Operations Table

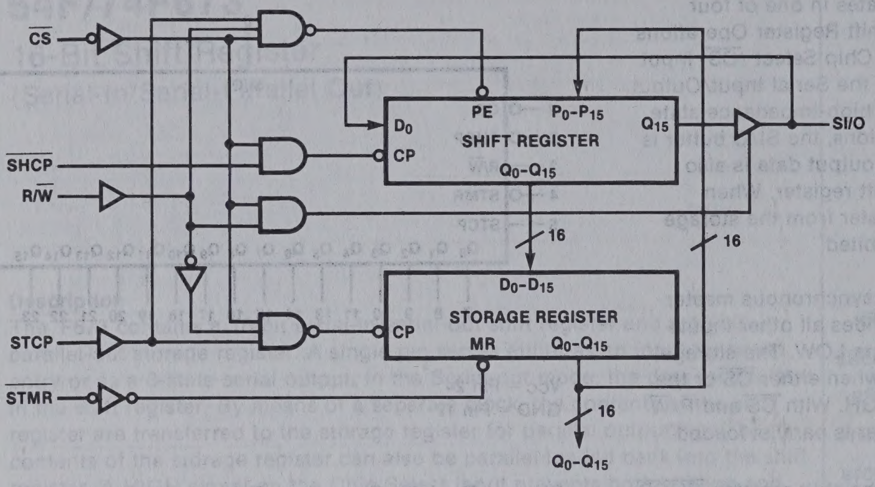
CONTROL INPUTS				OPERATING MODE
$\overline{STMR}$	$\overline{CS}$	R/$\overline{W}$	STCP	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

Shift Register Operations Table

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP		
H L	X L	X	X X	High Z Data In	Hold Serial Load
L	H	↓	L	Data Out	Serial Output with Recirculation
L	H	↓	H	Active	Parallel Load; No Shifting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram


CS
SHCP
R/W
STCP
STMR
D0
CP
PE
P0-P15
Q15
SHIFT REGISTER
Q0-Q15
SI/O
16
16
D0-D15
STORAGE REGISTER
CP
MR
Q0-Q15
16
Q0-Q15

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, SI/O			70	μA	$V_{IN} = 2.7$ V, V_{CC} = Max
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, SI/O			650	μA	$V_{IN} = 0.5$ V, V_{CC} = Max
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140						MHz	3-1, 3-8
t_{PLH}	Propagation Delay	7.5	13	18					ns	3-1
t_{PHL}	STCP to Q_n	9.5	16	22						3-7
t_{PHL}	Propagation Delay $\overline{\text{STMR}}$ to Q_n	6.0	10	14					ns	3-1 3-11
t_{PLH}	Propagation Delay	4.5	8.0	11					ns	3-1
t_{PHL}	$\overline{\text{SHCP}}$ to SI/O	5.0	9.0	12.5						3-8
t_{PZH}	Output Enable Time	3.0	5.0	7.0					ns	3-1 3-12 3-13
t_{PZL}	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to SI/O	3.0	5.0	7.0						
t_{PHZ}	Output Disable Time	3.0	5.0	7.0						
t_{PLZ}	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to SI/O	3.0	5.0	7.0						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	7.0							ns	3-5
t_s (L)	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to STCP	7.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to STCP	0								
t_s (H)	Setup Time, HIGH or LOW	3.0							ns	3-6
t_s (L)	SI/O to $\overline{\text{SHCP}}$	3.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	SI/O to $\overline{\text{SHCP}}$	0								
t_s (H)	Setup Time, HIGH or LOW	5.0							ns	3-6
t_s (L)	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to $\overline{\text{SHCP}}$	5.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	$\overline{\text{CS}}$ or R/$\overline{\text{W}}$ to $\overline{\text{SHCP}}$	0								
t_w (H)	$\overline{\text{SHCP}}$ Pulse Width,	4.0							ns	3-8
t_w (L)	HIGH or LOW	5.0								
t_w (H)	STCP Pulse Width,	5.0							ns	3-7
t_w (L)	HIGH or LOW	10								
t_w (L)	$\overline{\text{STMR}}$ Pulse Width LOW	7.0							ns	3-11
t_{rec}	Recovery Time $\overline{\text{STMR}}$ to STCP	10							ns	3-11

▨ Test limits in screened columns are preliminary.

54F/74F674

16-Bit Shift Register

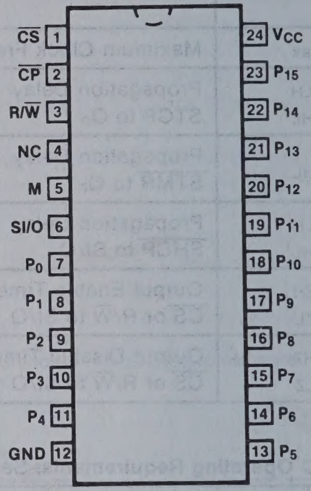
(Serial-Parallel-in/Serial-out)

Description

The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-state serial output. In the Serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-in/Serial-out Converter**
- **Recirculating Serial Shifting**
- **Common Serial Data I/O Pin**

Connection Diagram



$\overline{CS}$ 1
$\overline{CP}$ 2
$R/\overline{W}$ 3
NC 4
M 5
SI/O 6
P_0 7
P_1 8
P_2 9
P_3 10
P_4 11
GND 12
24 V_{CC}
23 P_{15}
22 P_{14}
21 P_{13}
20 P_{12}
19 P_{11}
18 P_{10}
17 P_9
16 P_8
15 P_7
14 P_6
13 P_5

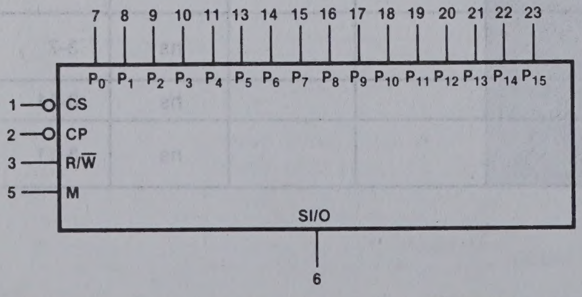
Ordering Code: See Section 6

Pkgs	Commercial Grade	Military Grade	Pkg Type
	V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	74F674PC		9N
Ceramic DIP (D)	74F674DC	54F674DM	6N
Flatpak (F)		54F674FM	4M

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
$P_0 - P_{15}$	Parallel Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active LOW)	0.5/0.375
M	Mode Select Input	0.5/0.375
$R/\overline{W}$	Read/Write Input	0.5/0.375
SI/O	3-State Serial Data Input or 3-State Serial Output	1.75/0.375 25/12.5

Logic Symbol



7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
P_0 P_1 P_2 P_3 P_4 P_5 P_6 P_7 P_8 P_9 P_{10} P_{11} P_{12} P_{13} P_{14} P_{15}
1 CS
2 CP
3 $R/\overline{W}$
5 M
SI/O
6

V_{CC} = Pin 24
GND = Pin 12

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold — a HIGH signal on the Chip Select ($\overline{\text{CS}}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high-impedance state.

Serial Load — data present on the SI/O pin shifts into the register on the falling edge of $\overline{\text{CP}}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output — the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load — data present on P_0 - P_{15} are entered into the register on the falling edge of $\overline{\text{CP}}$. The SI/O 3-state buffer is active and represents the Q_{15} output.

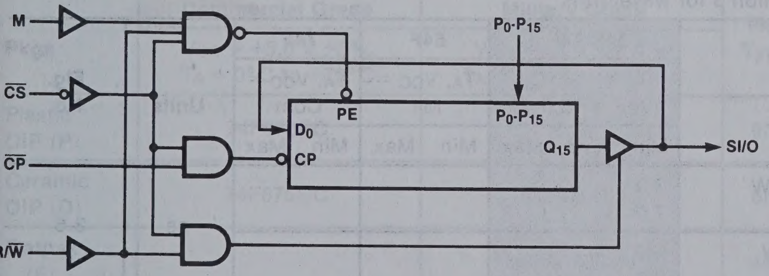
To prevent false clocking, $\overline{\text{CP}}$ must be LOW during a LOW-to-HIGH transition of $\overline{\text{CS}}$.

Shift Register Operations Table

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{\text{CS}}$	R/$\overline{\text{W}}$	M	$\overline{\text{CP}}$		
H L	X L	X X	X ⌐	High Z Data In	Hold Serial Load
L	H	L	⌐	Data Out	Serial Output with Recirculation
L	H	H	⌐	Active	Parallel Load; No Shifting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, SI/O			70	μA	$V_{IN} = 2.7$ V, V_{CC} = Max
$I_{IL} + I_{OZL}$	3-State Output OFF Current LOW, SI/O			650	μA	$V_{IN} = 0.5$ V, V_{CC} = Max
I_{CC}	Power Supply Current		53	80	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F ▨			54F		74F		Units	Fig. No.
		$T_A = +25°$C, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140						MHz	3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to SI/O	4.5 5.0	8.0 9.0	11 12.5					ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	3.0 3.0	5.0 5.0	7.0 7.0					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	3.0 3.0	5.0 5.0	7.0 7.0						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F ▨			54F		74F		Units	Fig. No.
		$T_A = +25°$C, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW SI/O to $\overline{CP}$	7.0 7.0							ns	3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW SI/O to $\overline{CP}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{CP}$	3.0 3.0							ns	3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{CP}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	5.0 5.0							ns	3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	0 0								
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width, HIGH or LOW	4.0 5.0							ns	3-8

▨ Test limits in screened columns are preliminary.

54F/74F675

16-Bit Shift Register

(Serial-in/Serial-Parallel Out)

Description

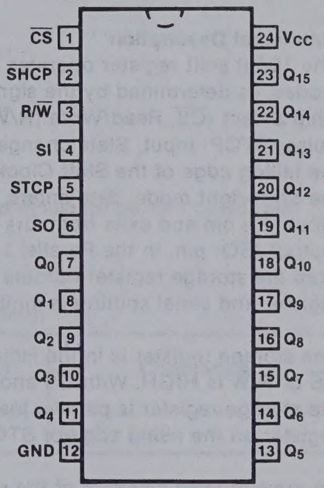
The 'F675 contains a 16-bit serial-in/serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-out Storage Register**
- **Recirculating Parallel Transfer**
- **Expandable for Longer Words**

Ordering Code: See Section 6

Pkgs	Commercial Grade V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	Military Grade V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	Pkg Type
Plastic DIP (P)	74F675PC		9N
Ceramic DIP (D)	74F675DC	54F675DM	6N
Flatpak (F)		54F675FM	4M

Connection Diagram

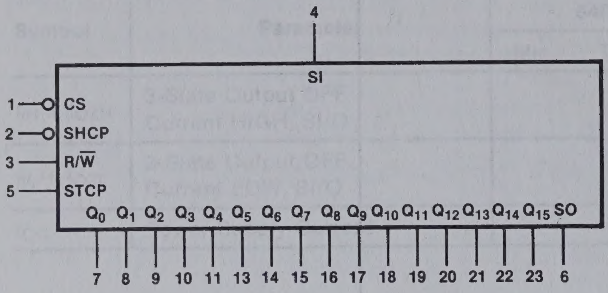


$\overline{CS}$ 1
$\overline{SHCP}$ 2
R/$\overline{W}$ 3
SI 4
STCP 5
SO 6
Q_0 7
Q_1 8
Q_2 9
Q_3 10
Q_4 11
GND 12
24 V_{CC}
23 Q_{15}
22 Q_{14}
21 Q_{13}
20 Q_{12}
19 Q_{11}
18 Q_{10}
17 Q_9
16 Q_8
15 Q_7
14 Q_6
13 Q_5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F (U.L.) HIGH/LOW
SI	Serial Data Input	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
STCP	Store Clock Pulse Input (Active Rising Edge)	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SO	Serial Data Output	25/12.5
$Q_0 - Q_{15}$	Parallel Data Outputs	25/12.5

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

Functional Description

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{\text{CS}}$), Read/Write (R/$\overline{\text{W}}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{\text{SHCP}}$). In the Shift-right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{\text{CS}}$ or R/$\overline{\text{W}}$ is HIGH. With $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{\text{SHCP}}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{\text{CS}}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{\text{CS}}$ if R/$\overline{\text{W}}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{\text{W}}$ if $\overline{\text{CS}}$ is LOW.

Shift Register Operations Table

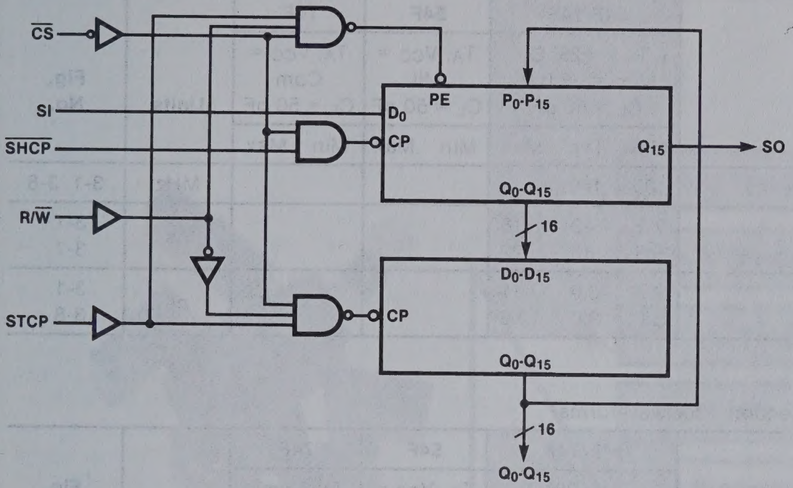
CONTROL INPUTS				OPERATING MODE
$\overline{\text{CS}}$	R/$\overline{\text{W}}$	$\overline{\text{SHCP}}$	STCP	
H	X	X	X	Hold
L	L	↓	X	Shift Right
L	H	↓	L	Shift Right
L	H	↓	H	Parallel Load; No Shifting

Storage Register Operations Table

INPUTS			OPERATING MODE
$\overline{\text{CS}}$	R/$\overline{\text{W}}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram


CS
SI
SHCP
R/W
STCP
PE
D0
CP
P0-P15
Q15
SO
Q0-Q15
16
D0-D15
CP
Q0-Q15
16
Q0-Q15

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

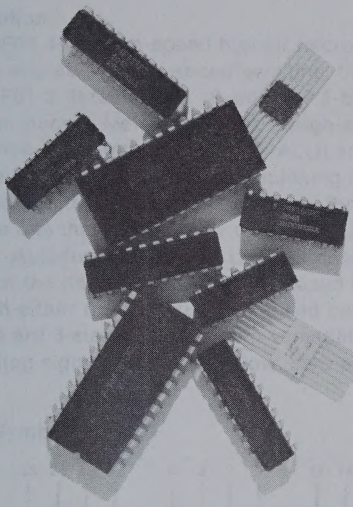
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°$ C, $V_{CC} = +5.0$ V $C_L = 50$ pF			T_A, V_{CC} = Mil $C_L = 50$ pF		T_A, V_{CC} = Com $C_L = 50$ pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140						MHz	3-1, 3-8
t_{PLH}	Propagation Delay	7.5	13	18					ns	3-1
t_{PHL}	STCP to Q_n	9.5	16	22						3-7
t_{PLH}	Propagation Delay	4.5	8.0	11					ns	3-1
t_{PHL}	$\overline{SHCP}$ to SO	5.0	9.0	12.5						3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°$ C, $V_{CC} = +5.0$ V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H)	Setup Time, HIGH or LOW	7.0							ns	3-5
t_s (L)	$\overline{CS}$ or R/$\overline{W}$ to STCP	7.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	$\overline{CS}$ or R/$\overline{W}$ to STCP	0								
t_s (H)	Setup Time, HIGH or LOW	3.0							ns	3-6
t_s (L)	SI to $\overline{SHCP}$	3.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	SI to $\overline{SHCP}$	0								
t_s (H)	Setup Time, HIGH or LOW	5.0							ns	3-6
t_s (L)	R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	5.0								
t_h (H)	Hold Time, HIGH or LOW	0								
t_h (L)	R/$\overline{W}$ or $\overline{CS}$ to $\overline{SHCP}$	0								
t_w (H)	$\overline{SHCP}$ Pulse Width,	4.0							ns	3-8
t_w (L)	HIGH or LOW	5.0								
t_w (H)	STCP Pulse Width,	5.0							ns	3-7
t_w (L)	HIGH or LOW	10								

▨ Test limits in screened columns are preliminary.



Product Index and Selection Guide 1

Circuit Characteristics 2

Ratings, Specifications and Waveforms 3

Data Sheets 4

New Products 5

Ordering Information and Package Outlines 6

Sales Offices, Representatives and Distributor Locations 7

29F01

4-Bit Bipolar Microprocessor Slice

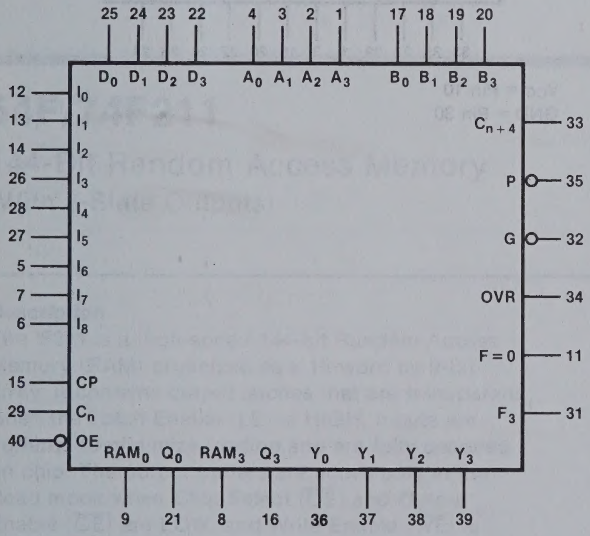
Description

The 29F01 4-bit high-speed bipolar microprocessor slice is available in two speed versions, the 29F01-1 and 29F01-2. It features a 16-word by 4-bit dual-port Random Access Memory (RAM), a high-speed 8-function Arithmetic Logic Unit (ALU) and associated shifting, decoding and multiplexing circuitry. The microinstruction word consists of three groups of three bits that respectively control ALU operand source, ALU function and ALU result destination. Width of the data path may be increased by cascading with either ripple or full lookahead carry. Data outputs are 3-state for maximum versatility. Four status flag signals, carry, overflow, zero and sign, are provided by the ALU. The microprocessor slice is compatible with Fairchild Advanced Schottky TTL (FAST) devices and can be used with FAST parts in microprogrammed systems to minimize cycle times.

The 29F01-1 and 29F01-2 are plug-in replacements for the 2901 series microprocessors.

Isoplanar FAST Technology
Plug-in Replacement for Standard 2901
20% to 30% Faster than Standard 2901 in Most System Configurations
Clock Pulse LOW Time 20 ns

Logic Symbol


25 24 23 22 4 3 2 1 17 18 19 20
D_0 D_1 D_2 D_3 A_0 A_1 A_2 A_3 B_0 B_1 B_2 B_3
12 I_0
13 I_1
14 I_2
26 I_3
28 I_4
27 I_5
5 I_6
7 I_7
6 I_8
15 CP
29 C_n
40 OE
C_{n+4} 33
P 35
G 32
OVR 34
F = 0 11
F_3 31
RAM_0 Q_0 RAM_3 Q_3 Y_0 Y_1 Y_2 Y_3
9 21 8 16 36 37 38 39

V_{CC} = Pin 10
GND = Pin 30

29F10

Microprogram Controller

Description

The 29F10 is a high-speed bipolar microprogram controller. It is intended for use in controlling the execution sequence of microinstructions stored in microprogram memory. The 29F10 provides a 12-bit address during each clock cycle. This address comes from one of four sources: direct input from D_0-D_{11}, the Register/Counter, the Microprogram Counter-Register, or the 5-deep LIFO Stack. Address outputs are 3-state for maximum versatility.

The microprogram controller is compatible with Fairchild Advanced Schottky TTL (FAST) devices and can be used with FAST parts in microprogrammed systems to minimize cycle times.

Addresses up to 4096 Words of Microcode

Directly Loadable Down-counter for Counting Loop Iterations

Provides Count Capacity of 4096

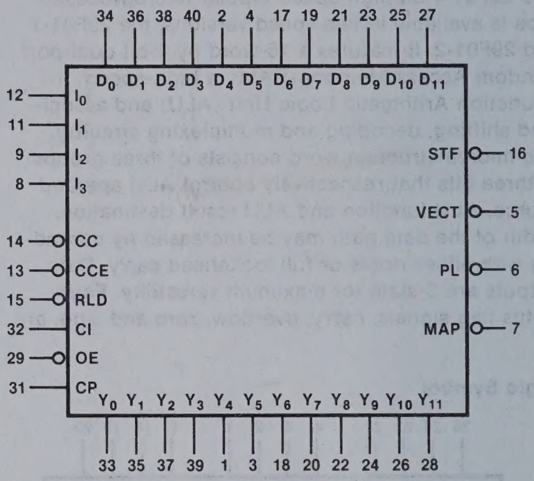
Up-counter Provides Sequential Microinstruction Execution

5-Deep Push/Pop LIFO Stack Provides Subroutine Linkage and Branch Capabilities

All Registers Positive Edge-triggered

Plug-in Replacement for Standard 2910

Logic Symbol


34 36 38 40 2 4 17 19 21 23 25 27
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9 D_{10} D_{11}
12 I_0
11 I_1
9 I_2
8 I_3
14 CC
13 CCE
15 RLD
32 CI
29 OE
31 CP
STF 16
VECT 5
PL 6
MAP 7
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7 Y_8 Y_9 Y_{10} Y_{11}
33 35 37 39 1 3 18 20 22 24 26 28

V_{CC} = Pin 10

GND = Pin 30

29F705

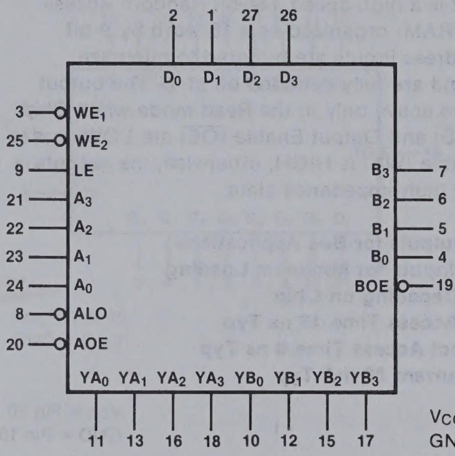
16-Word by 4-Bit
2-Port Random Access Memory

Description

The 29F705 is a 16-word by 4-bit Random Access Memory (RAM). It provides two separate output ports to allow simultaneous reading of any two 4-bit words, and has 3-state outputs for bussing.

High-speed Version of 29705
16-Word by 4-Bit, 2-Port RAM
Separate 4-Bit Latches on Each Output Port
3-State Outputs

Logic Symbol


2
1
27
26
D0
D1
D2
D3
3
WE1
25
WE2
9
LE
21
A3
22
A2
23
A1
24
A0
8
ALO
20
AOE
B3
7
B2
6
B1
5
B0
4
BOE
19
YA0
YA1
YA2
YA3
YB0
YB1
YB2
YB3
11
13
16
18
10
12
15
17

V_{CC} = Pin 28
GND = Pin 14

54F/74F211

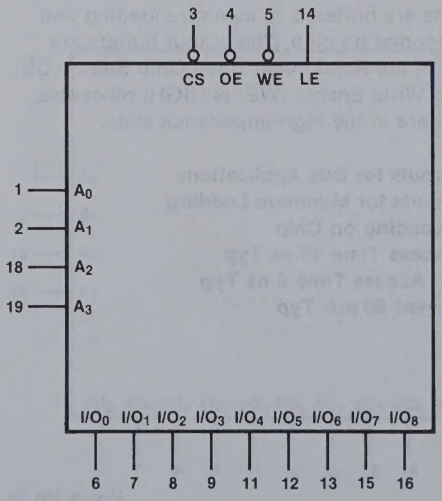
144-Bit Random Access Memory
(With 3-State Outputs)

Description

The 'F211 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. It contains output latches that are transparent when the Latch Enable (LE) is HIGH. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) are LOW, and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

3-State Outputs for Bus Applications
Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

Logic Symbol


3
4
5
14
CS
OE
WE
LE
1
A0
2
A1
18
A2
19
A3
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
6
7
8
9
11
12
13
15
16

V_{CC} = Pin 20
GND = Pin 10

54F/74F212

144-Bit Random Access Memory

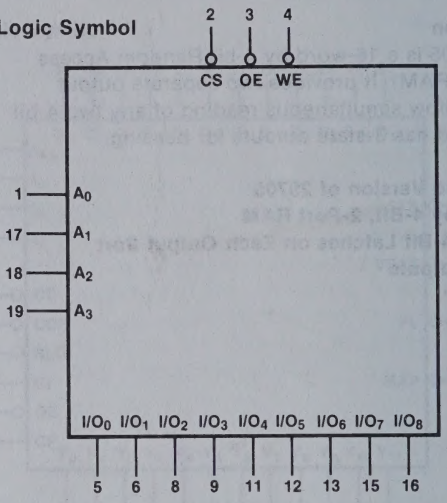
(With 3-State Outputs)

Description

The 'F212 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) are LOW, and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

3-State Outputs for Bus Applications
Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

Logic Symbol



2
3
4
CS
OE
WE
1
17
18
19
A_0
A_1
A_2
A_3
I/O_0 I/O_1 I/O_2 I/O_3 I/O_4 I/O_5 I/O_6 I/O_7 I/O_8
5 6 8 9 11 12 13 15 16

V_{CC} = Pin 20
GND = Pin 10

54F/74F213

192-Bit Random Access Memory

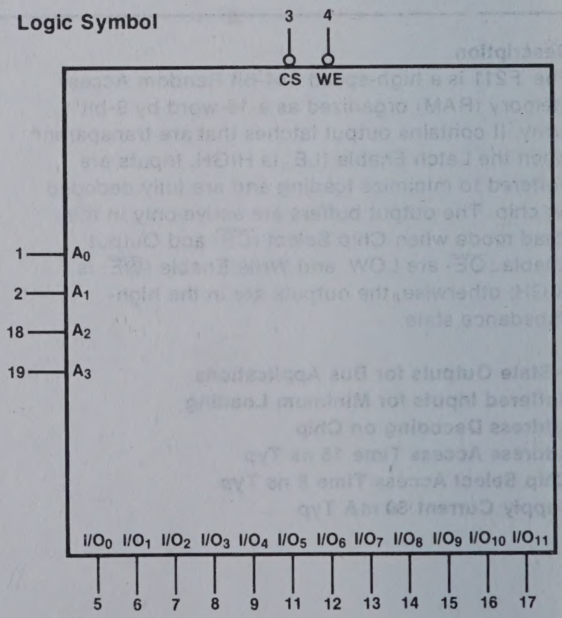
(With 3-State Outputs)

Description

The 'F213 is a high-speed 192-bit Random Access Memory (RAM) organized as a 16-word by 12-bit array. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) is LOW and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

3-State Outputs for Bus Applications
Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

Logic Symbol



3
4
CS
WE
1
2
18
19
A_0
A_1
A_2
A_3
I/O_0 I/O_1 I/O_2 I/O_3 I/O_4 I/O_5 I/O_6 I/O_7 I/O_8 I/O_9 I/O_{10} I/O_{11}
5 6 7 8 9 11 12 13 14 15 16 17

V_{CC} = Pin 20
GND = Pin 10

54F/74F269

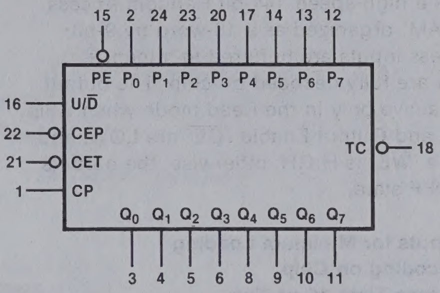
8-Bit Bidirectional Binary Counter

Description

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Synchronous Counting and Loading
Built-in Lookahead Carry Capability
Count Frequency 100 MHz Typ
Supply Current 70 mA Typ

Logic Symbol


15
2
24
23
20
17
14
13
12
PE
P_0
P_1
P_2
P_3
P_4
P_5
P_6
P_7
16
U/$\overline{D}$
22
CEP
21
CET
1
CP
TC
18
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
3
4
5
6
8
9
10
11

V_{CC} = Pin 19
GND = Pin 7

54F/74F311

144-Bit Random Access Memory

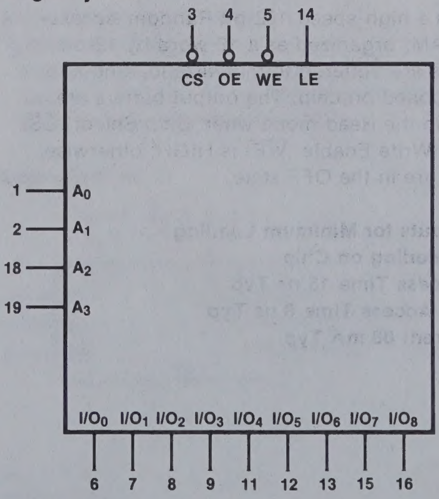
(With Open-collector Outputs)

Description

The 'F311 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. It contains output latches that are transparent when the Latch Enable (LE) is HIGH. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) are LOW, and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the OFF state.

Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

Logic Symbol


3
4
5
14
CS
OE
WE
LE
1
A_0
2
A_1
18
A_2
19
A_3
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
I/O_8
6
7
8
9
11
12
13
15
16

V_{CC} = Pin 20
GND = Pin 10

54F/74F312

144-Bit Random Access Memory

(With Open-collector Outputs)

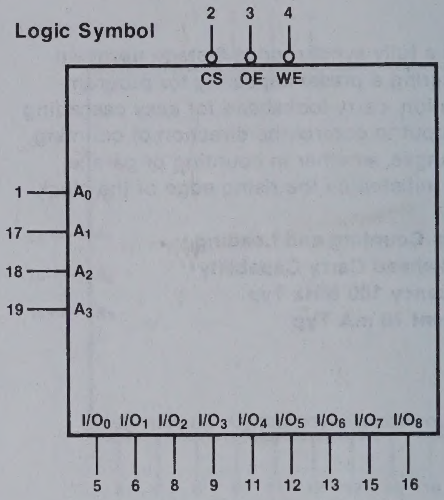
Description

The 'F312 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{\text{CS}}$) and Output Enable ($\overline{\text{OE}}$) are LOW, and Write Enable ($\overline{\text{WE}}$) is HIGH; otherwise, the outputs are in the OFF state.

Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

V_{CC} = Pin 20
GND = Pin 10

Logic Symbol


2
3
4
CS
OE
WE
1
A0
17
A1
18
A2
19
A3
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
5
6
8
9
11
12
13
15
16

54F/74F313

192-Bit Random Access Memory

(With Open-collector Outputs)

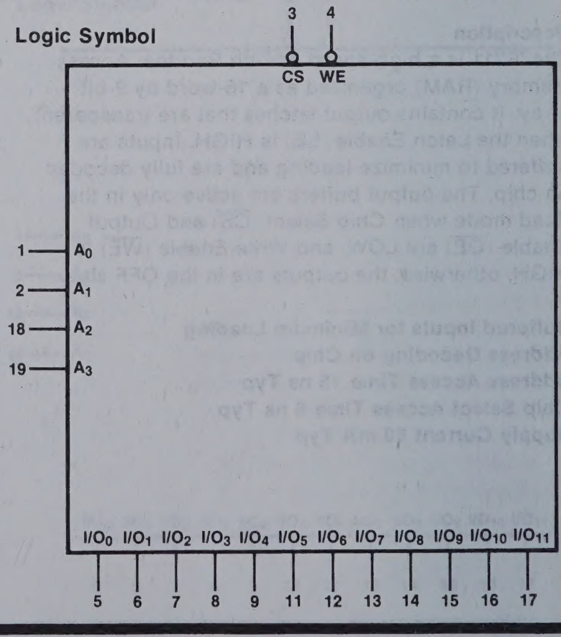
Description

The 'F313 is a high-speed 192-bit Random Access Memory (RAM) organized as a 16-word by 12-bit array. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{\text{CS}}$) is LOW and Write Enable ($\overline{\text{WE}}$) is HIGH; otherwise, the outputs are in the OFF state.

Buffered Inputs for Minimum Loading
Address Decoding on Chip
Address Access Time 15 ns Typ
Chip Select Access Time 8 ns Typ
Supply Current 80 mA Typ

V_{CC} = Pin 20
GND = Pin 10

Logic Symbol


3
4
CS
WE
1
A0
2
A1
18
A2
19
A3
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
I/O10
I/O11
5
6
7
8
9
11
12
13
14
15
16
17

54F/74F401

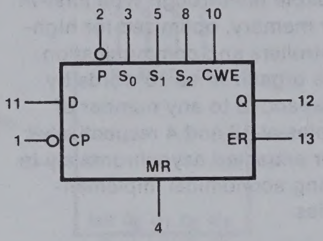
Cyclic Redundancy Check Generator/Checker

Description

The 'F401 Cyclic Redundancy Check (CRC) generator/checker implements the most widely used error detection scheme in serial digital data handling systems. On transmission, the data stream is encoded by dividing it by a set polynomial. The remainder is appended to the message as check bits. Upon reception, this data stream is divided by the same polynomial and if there is no remainder, there are no detectable errors.

Eight Selectable Polynomials
Error Indicator
More Efficient than Parity in Checking Errors
High-speed Data Rate
Supply Current 70 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

54F/74F402

Expandable Cyclic Redundancy Check Generator/Checker

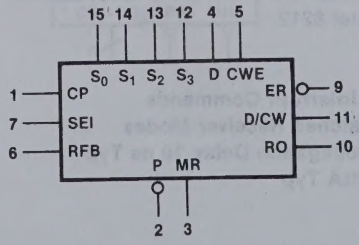
Description

The 'F402 expandable Cyclic Redundancy Check (CRC) generator/checker is an expandable version of the 'F401. It provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital handling systems. A 4-bit control input selects one-of-six generator polynomials. The list of polynomials includes CRC-16, CRC-CCITT and Ethernet, as well as three other standard polynomials (56th order, 48th order, 32nd order). Individual clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. The CWG Control input inhibits feedback during check word transmission. The 'F402 is compatible with Fairchild Advanced Schottky TTL (FAST) devices and is fully compatible with all TTL families.

Guaranteed 20 MHz Data Rate
Six Selectable Polynomials
Other Polynomials Available
Separate Preset and Clear Controls

Expandable
Automatic Right Justification
Error Output Open Collector
Typical Applications
  Floppy and Other Disk Storage Systems
  Digital Cassette and Cartridge Systems
  Data Communication Systems

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

54F/74F403

16 X 4 First-In First-Out Buffer Memory

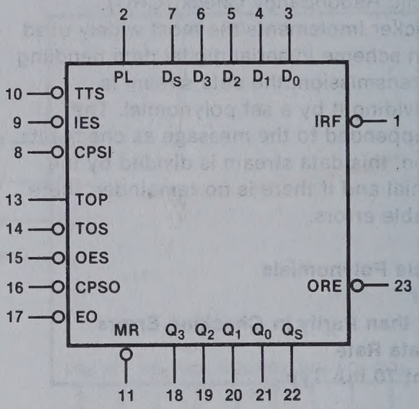
(With 3-State Outputs)

Description

The 'F403 is an expandable fall-through type First-In First-Out (FIFO) buffer memory, optimized for high-speed disk or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or bits (in multiples of 16 and 4 respectively). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

- **Serial or Parallel Data Rate 10 MHz**
- **Serial or Parallel Input/Output**
- **Expandable in Width and Depth**
- **3-State Outputs**
- **Supply Current 115 mA Typ**

Logic Symbol


2
7
6
5
4
3
PL
D_S
D_3
D_2
D_1
D_0
10
TTS
9
IES
8
CPSI
13
TOP
14
TOS
15
OES
16
CPSO
17
EO
IRF
1
ORE
23
MR
Q_3
Q_2
Q_1
Q_0
Q_S
11
18
19
20
21
22

V_{CC} = Pin 24
GND = Pin 12

54F/74F412

Multi-mode Buffered Latch

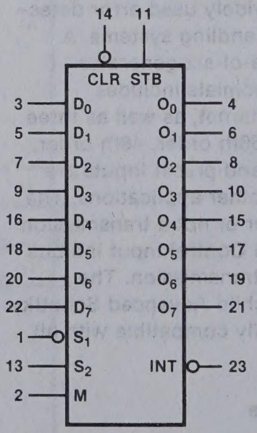
(With 3-State Outputs)

Description

The 'F412 is an 8-bit latch with 3-state output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode. The 'F412 is the functional equivalent of the Intel 8212.

- **3-State Outputs**
- **Status Flip-flop for Interrupt Commands**
- **Asynchronous or Latched Receiver Modes**
- **Select to Output Propagation Delay 10 ns Typ**
- **Supply Current 43 mA Typ**

Logic Symbol


14
11
CLR
STB
3
D_0
O_0
4
5
D_1
O_1
6
7
D_2
O_2
8
9
D_3
O_3
10
16
D_4
O_4
15
18
D_5
O_5
17
20
D_6
O_6
19
22
D_7
O_7
21
1
S_1
13
S_2
INT
23
2
M

V_{CC} = Pin 24
GND = Pin 12

54F/74F413

64 X 4 First-In First-Out Buffer Memory

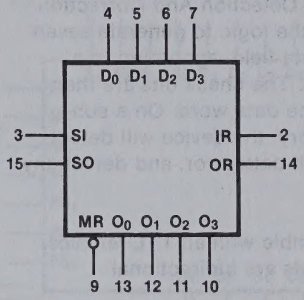
(With Serial and Parallel I/O)

Description

The 'F413 is an expandable fall-through type high-speed First-In First-Out (FIFO) buffer memory organized as 64 words by four bits. The 4-bit input and output registers record and transmit, respectively, asynchronous data in either serial or parallel form. Control pins on the input and output allow for handshaking and expansion. The 4-bit wide, 62-bit deep fall-through stack has self-contained control logic. The outputs are in the high-impedance state when the Output Enable is HIGH.

Separate Input and Output Clocks
Serial or Parallel Input and Output
Expandable without External Logic
15 MHz Data Rate
Supply Current 115 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

54F/74F416

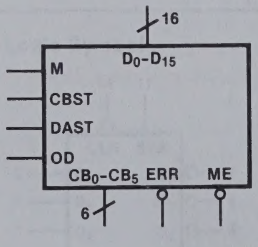
16-Bit Memory Error Detection And Correction Circuit

Description

The 'F416 memory Error Detection And Correction (EDAC) circuit contains the logic to generate six check bits on a 16-bit data field, according to a modified Hamming code. The check bits are then stored in memory with the data word. On a subsequent read from memory, the device will detect and correct any single-bit data error, and detect any double-bit error. The 'F416 is a 16-bit version of the 'F418.

Increases Memory System Reliability
Corrects Single-bit Errors
Detects Double-bit Errors

Logic Symbol



54F/74F418

32-Bit Memory Error Detection And Correction Circuit

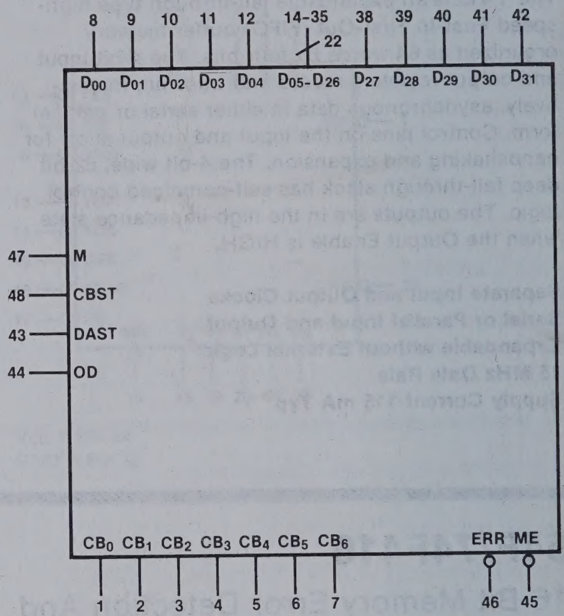
Description

The 'F418 memory Error Detection And Correction (EDAC) circuit contains the logic to generate seven check bits on a 32-bit data field, according to a modified Hamming code. The check bits are then stored in memory with the data word. On a subsequent read from memory, the device will detect and correct any single-bit data error, and detect any double-bit error.

The 'F418 is fully compatible with all TTL families. Data and check-bit signals are bidirectional 3-state lines.

Increases Memory System Reliability
Corrects Single-bit Errors in 60 ns
Detects Double-bit Errors in 65 ns

Logic Symbol


8
9
10
11
12
14–35
22
38
39
40
41
42
D_{00}
D_{01}
D_{02}
D_{03}
D_{04}
D_{05}-D_{26}
D_{27}
D_{28}
D_{29}
D_{30}
D_{31}
47 M
48 CBST
43 DAST
44 OD
CB_0
CB_1
CB_2
CB_3
CB_4
CB_5
CB_6
ERR
ME
1
2
3
4
5
6
7
46
45

V_{CC} = Pin 36
GND = Pins 13, 37

54F/74F430

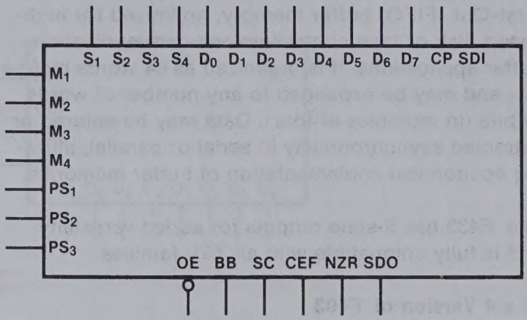
Cyclic Redundancy Checker/Corrector

Description

The 'F430 Cyclic Redundancy Checker/Corrector (CRCC) is a serial burst-error detection/correction circuit, using a 32-order polynomial selected by internal Read Only Memory (ROM). When used at the data transmission source, the 'F430 generates a cyclic redundancy check code and appends it to a data block transmission. When the device is placed at the receiving end of a transmission, it is used to verify the integrity of the data block that now contains the appended check code. Should an error be detected, under user control, the device can be made to correct the bits in error. The CRCC is used in high-performance serial data transmission applications such as disk and tape controllers, as well as communications equipment and serial data interfaces between mainframes and peripherals.

Eight Different Polynomials, up to 32nd Order (e.g. Ethernet)
Clocking Rate 25 MHz
28-Pin Package

Logic Symbol



54F/74F432

Multi-mode Buffered Latch

(With 3-State Outputs)

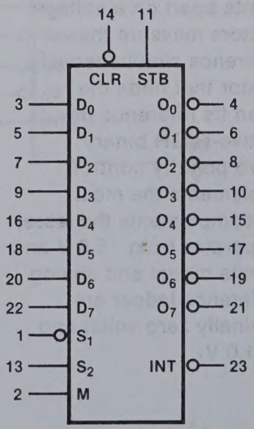
Description

The 'F432 is an 8-bit latch with 3-state output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode.

The 'F432 is the functional equivalent of the Intel 8212, but with inverting outputs.

3-State Inverting Outputs
Status Flip-flop for Interrupt Commands
Asynchronous or Latched Receiver Modes
Select to Output Propagation Delay 10 ns
Supply Current 43 mA Typ

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

54F/74F433

64 x 4 First-In First-Out Buffer Memory

(With 3-State Outputs)

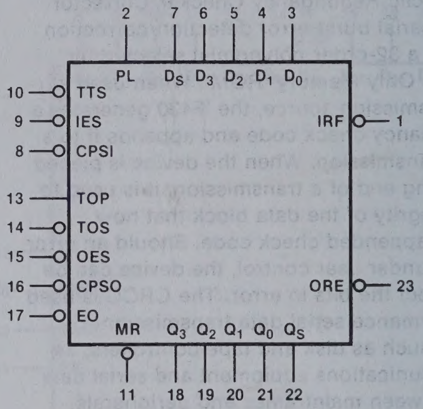
Description

The 'F433 is an expandable fall-through type First-In First-Out (FIFO) buffer memory, optimized for high-speed disk or tape controllers and communication buffer applications. It is organized as 64 words by four bits and may be expanded to any number of words or bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 'F433 has 3-state outputs for added versatility and is fully compatible with all TTL families.

64 x 4 Version of 'F403
Serial or Parallel Input/Output
Expandable without External Logic
Serial or Parallel Data Rate 10 MHz
24-Pin Package

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

54F/74F500

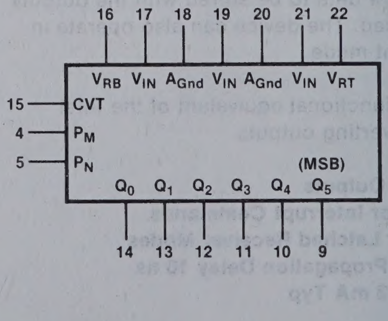
6-Bit Analog-to-Digital Converter

Description

The 'F500 is a 6-bit, fully parallel analog-to-digital converter capable of sampling at rates from 0 to 50 MHz. Conversion is accomplished by 64 comparators spaced one quanta apart on a voltage reference ladder. All comparators measure the analog input against their reference simultaneously. The most significant comparator that finds the analog input to be greater than its reference has its output encoded to a 6-bit, active-HIGH binary number, stored in latches. Two polarity control inputs are provided: P_M complements the most significant output bit and P_N complements the lesser five output bits. The circuit operates from +5.0 V and -6.0 V supplies and has separate digital and analog grounds. Both ends of the reference ladder are brought out, one to V_{RT} (nominally zero volts) and the other to V_{RB} (nominally -1.0 V).

No Sample and Hold Required
Sampling Rate 40 MHz Typ
Aperture Time 4.0 ns Typ
V_{CC} Supply Current 20 mA Typ
V_{EE} Supply Current 102 mA Typ

Logic Symbol



V_{CC} = Pin 7
V_{EE} = Pins 1, 6
D_{Gnd} = Pin 8

54F/74F505

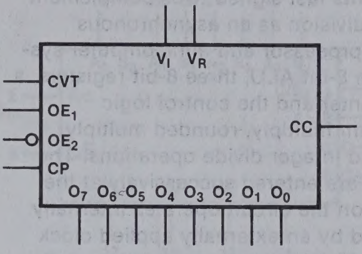
8-Bit Analog-to-Digital Converter

Description

The 'F505 is an 8-bit A-to-D converter using the successive approximation technique. It contains an 8-bit successive approximation shift register connected internally to an 8-bit D-to-A converter. The converter output drives one input of an on-chip analog comparator. The 'F505 is intended for use where the speed of flash converters is not needed. Its handshaking facilities and 3-state outputs make it microprocessor compatible.

8-Bit Resolution
Single 5 V Power Supply Required
Input Range 0.2 V
Conversion Time 200 ns Typ
Clock Frequency 40 MHz Typ

Logic Symbol



V_I
V_R
CVT
OE_1
OE_2
CP
CC
O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0

54F/74F525

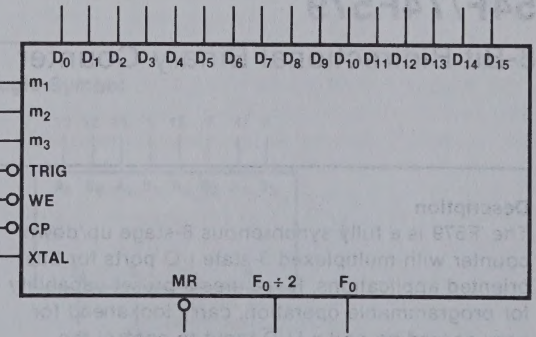
16-Stage Programmable Counter/Timer

Description

The 'F525 is a 16-bit multimode programmable timer, divider, and frequency generator. It incorporates a 16-bit presettable counter, a 16-bit latch, crystal oscillator circuit and control circuitry. Modes include programmable timer, divider, one shot and terminal count interrupt.

28-Pin Package
16-Stage Divider
Clock Frequency 50 MHz Typ
Supply Current 100 mA Typ

Logic Symbol



D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9 D_{10} D_{11} D_{12} D_{13} D_{14} D_{15}
m_1
m_2
m_3
TRIG
WE
CP
XTAL
MR
$F_0 \div 2$
F_0

54F/74F559

Expandable 8-Bit Twos Complement Multiplier/Divider

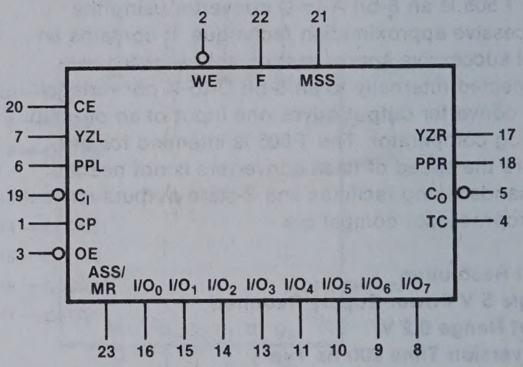
(With 3-State Outputs)

Description

The 'F559 implements fast signed twos complement multiplication and division as an asynchronous peripheral in microprocessor and minicomputer systems. It contains an 8-bit ALU, three 8-bit registers, a 4-bit sequence counter and the control logic necessary to perform multiply, rounded multiply, fractional divide and integer divide operations. The two 8-bit operands are entered successively at the I/O ports, whereupon the circuit operates internally at a rate determined by an externally applied clock frequency of up to 25 MHz. Upon completion, and upon command, results are presented at the I/O ports in successive 8-bit words. Linking inputs and outputs are provided for expansion to longer words by using two or more multipliers operating on the same 8-bit bus.

Signed Twos Complement Arithmetic
Increases Processor Efficiency
Low System Parts Count
Expandable in 8-Bit Increments
8-Bit Bus Oriented 3-State I/O
16-Bit Multiply in 1.2 μs Typ
16-Bit Divide in 1.6 μs Typ

Logic Symbol


2
22
21
WE
F
MSS
20
CE
7
YZL
6
PPL
19
C_I
1
CP
3
OE
YZR
17
PPR
18
C_O
5
TC
4
ASS/MR
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
23
16
15
14
13
11
10
9
8

V_{CC} = Pin 24
GND = Pin 12

54F/74F579

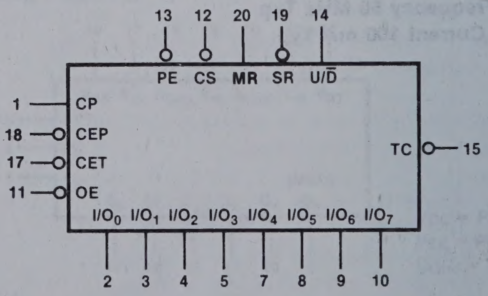
8-Bit Bidirectional Binary Counter

Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a $U/\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Multiplexed 3-state I/O Ports
Space Saving 20-Pin Package
Built-in Lookahead Carry Capability
Count Frequency 100 MHz Typ
Supply Current 75 mA Typ

Logic Symbol


13
12
20
19
14
PE
CS
MR
SR
$U/\overline{D}$
1
CP
18
CEP
17
CET
11
OE
TC
15
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
2
3
4
5
7
8
9
10

V_{CC} = Pin 16
GND = Pin 6

54F/74F582

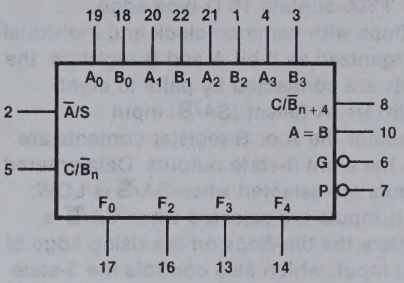
4-Bit BCD Arithmetic Logic Unit

Description

The 'F582 is a 24-pin expandable Arithmetic Logic Unit (ALU) that performs two arithmetic operations (A plus B, A minus B), compare (A equals B), and binary to BCD conversion. In addition to a ripple carry output, carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to higher decades. It is functionally equivalent to the 82S82.

- **24-Pin Package**
- **Performs Four BCD Functions**
- **$\overline{P}$ and $\overline{G}$ Outputs for High-speed Expansion**
- **Add/Subtract Delay 14 ns Typ**
- **Lookahead Delay 12 ns Typ**
- **Supply Current 55 mA Typ**

Logic Symbol


19 18 20 22 21 1 4 3
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
2
$\overline{A}/S$
$C/\overline{B}_{n+4}$
8
$A = B$
10
5
$C/\overline{B}_n$
G
6
P
7
F_0 F_2 F_3 F_4
17 16 13 14

V_{CC} = Pin 24
GND = Pin 12

54F/74F583

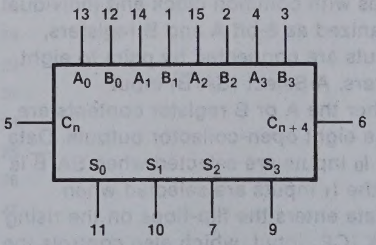
4-Bit BCD Adder

Description

The 'F583 high-speed 4-bit BCD full adder with internal carry lookahead accepts two 4-bit decimal numbers ($A_0 - A_3$, $B_0 - B_3$) and a Carry Input (C_n). It generates the decimal sum outputs ($S_0 - S_3$), and a Carry Output (C_{n+4}) if the sum is greater than 9. The 'F583 is the functional equivalent of the 82S83.

- **Adds Two Decimal Numbers**
- **Full Internal Lookahead**
- **Fast Ripple Carry for Economical Expansion**
- **Sum Output Delay Time 11 ns Typ**
- **Ripple Carry Delay Time 6 ns Typ**
- **Input to Ripple Delay Time 9 ns Typ**
- **Supply Current 50 mA Typ**

Logic Symbol


13 12 14 1 15 2 4 3
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
5
C_n
C_{n+4}
6
S_0 S_1 S_2 S_3
11 10 7 9

V_{CC} = Pin 16
GND = Pin 8

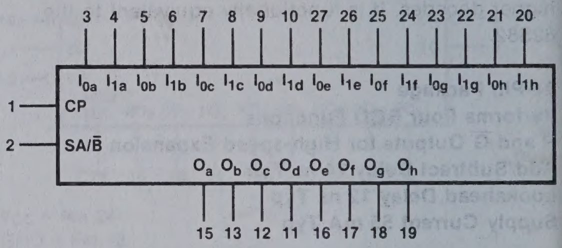
54F/74F604
54F/74F606
Dual Octal Registers
(With Multiplexed 3-State Outputs)

Description
The 'F604 and 'F606 contain 16 D-type edge-triggered flip-flops with common clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select ($SA/\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight 3-state outputs. Data entered from the I_0 inputs are selected when $SA/\overline{B}$ is LOW; data from the I_1 inputs are selected when $SA/\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the 3-state outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

These functions are well suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words. The 'F606 has glitch-free outputs; the 'F604 has reduced propagation delays.

Stores 16-Bit Wide Data Inputs
Multiplexed 8-Bit Outputs
High-speed or Glitch-free Version
3-State Outputs
Propagation Delay 10 ns Typ
Power Supply Current 140 mA Typ

Logic Symbol


3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20
I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d} I_{0e} I_{1e} I_{0f} I_{1f} I_{0g} I_{1g} I_{0h} I_{1h}
1 CP
2 $SA/\overline{B}$
O_a O_b O_c O_d O_e O_f O_g O_h
15 13 12 11 16 17 18 19

V_{CC} = Pin 28
GND = Pin 14

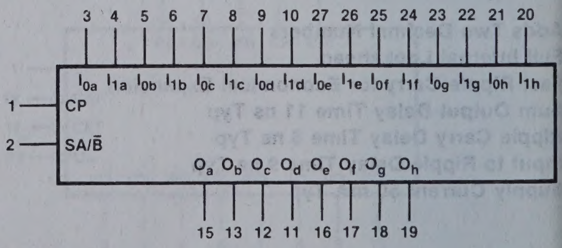
54F/74F605
54F/74F607
Dual Octal Registers
(With Multiplexed Open-collector Outputs)

Description
The 'F605 and 'F607 contain 16 D-type edge-triggered flip-flops with common clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select ($SA/\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight open-collector outputs. Data entered from the I_0 inputs are selected when $SA/\overline{B}$ is LOW; data from the I_1 inputs are selected when $SA/\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the open-collector outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

These functions are well suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words. The 'F607 has glitch-free outputs; the 'F605 has reduced propagation delays.

Stores 16-Bit Wide Data Inputs
Multiplexed 8-Bit Outputs
High-speed or Glitch-free Version
Open-collector Outputs
Propagation Delay 10 ns Typ
Power Supply Current 140 mA Typ

Logic Symbol


3 4 5 6 7 8 9 10 27 26 25 24 23 22 21 20
I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d} I_{0e} I_{1e} I_{0f} I_{1f} I_{0g} I_{1g} I_{0h} I_{1h}
1 CP
2 $SA/\overline{B}$
O_a O_b O_c O_d O_e O_f O_g O_h
15 13 12 11 16 17 18 19

V_{CC} = Pin 28
GND = Pin 14

54F/74F610

Memory Mapper
(With 3-State Outputs and Output Latches)

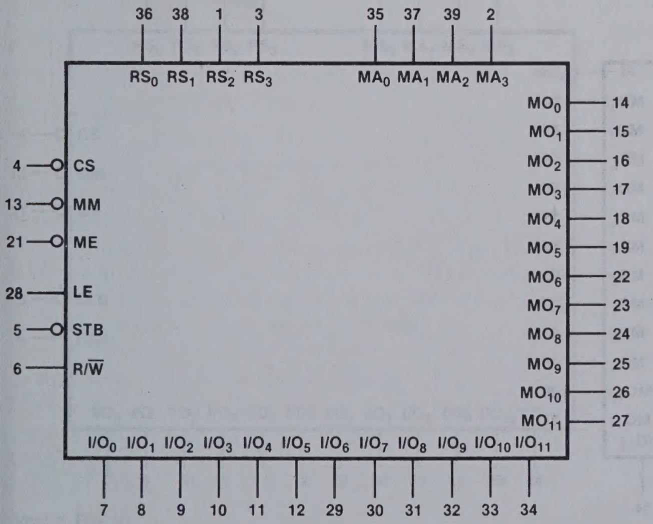
Description

The 'F610 memory mapper is designed to expand the address capability of a Central Processing Unit (CPU) by eight bits. The device contains 16 map registers, each containing 12 bits, that are loaded by the CPU. Subsequently, the four most significant bits of the memory address select one of the 16 registers. The 12 output bits, plus the four least significant memory address bits, form the expanded address. In this mode the 'F610 output stages may be transparent or latched. The addressable memory space is increased by periodically reloading the map registers.

In the pass mode the address bits on the register select inputs appear as the most significant bits at the map outputs, with LOW levels appearing on the other bit positions.

Increases Addressing Capability by Eight Bits
Designed for Paged Memory Mapping
Output Latches
3-State Outputs

Logic Symbol


36
38
1
3
35
37
39
2
RS_0
RS_1
RS_2
RS_3
MA_0
MA_1
MA_2
MA_3
4 CS
13 MM
21 ME
28 LE
5 STB
6 R/$\overline{W}$
MO_0 14
MO_1 15
MO_2 16
MO_3 17
MO_4 18
MO_5 19
MO_6 22
MO_7 23
MO_8 24
MO_9 25
MO_{10} 26
MO_{11} 27
I/O_0 7
I/O_1 8
I/O_2 9
I/O_3 10
I/O_4 11
I/O_5 12
I/O_6 29
I/O_7 30
I/O_8 31
I/O_9 32
I/O_{10} 33
I/O_{11} 34

V_{CC} = Pin 40
GND = Pin 20

54F/74F611

Memory Mapper

(With Open-collector Outputs and Output Latches)

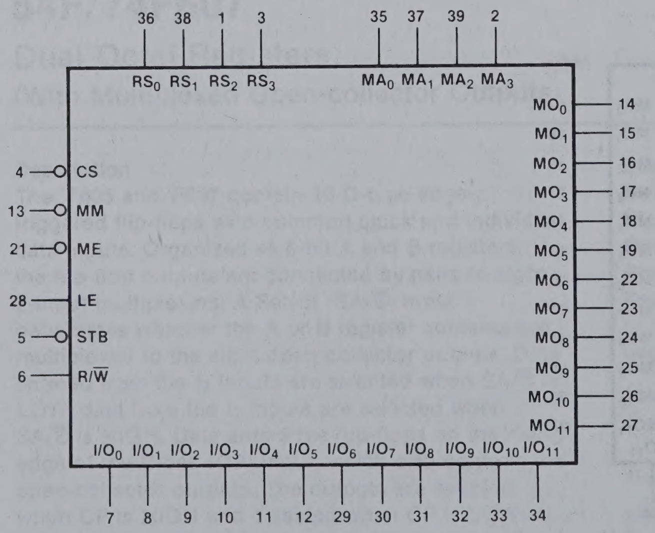
Description

The 'F611 memory mapper is designed to expand the address capability of a Central Processing Unit (CPU) by eight bits. The device contains 16 map registers, each containing 12 bits, that are loaded by the CPU. Subsequently, the four most significant bits of the memory address select one of the 16 registers. The 12 output bits, plus the four least significant memory address bits, form the expanded address. In this mode the 'F611 output stages may be transparent or latched. The addressable memory space is increased by periodically reloading the map registers.

In the pass mode the address bits on the register select inputs appear as the most significant bits at the map outputs, with LOW levels appearing on the other bit positions.

Increases Addressing Capability by Eight Bits
Designed for Paged Memory Mapping
Output Latches
Open-collector Outputs

Logic Symbol


36
38
1
3
35
37
39
2
RS0 RS1 RS2 RS3
MA0 MA1 MA2 MA3
MO0 14
MO1 15
MO2 16
MO3 17
MO4 18
MO5 19
MO6 22
MO7 23
MO8 24
MO9 25
MO10 26
MO11 27
4 CS
13 MM
21 ME
28 LE
5 STB
6 R/W
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9 I/O10 I/O11
7 8 9 10 11 12 29 30 31 32 33 34

V_{CC} = Pin 40
GND = Pin 20

54F/74F612

Memory Mapper

(With 3-State Outputs)

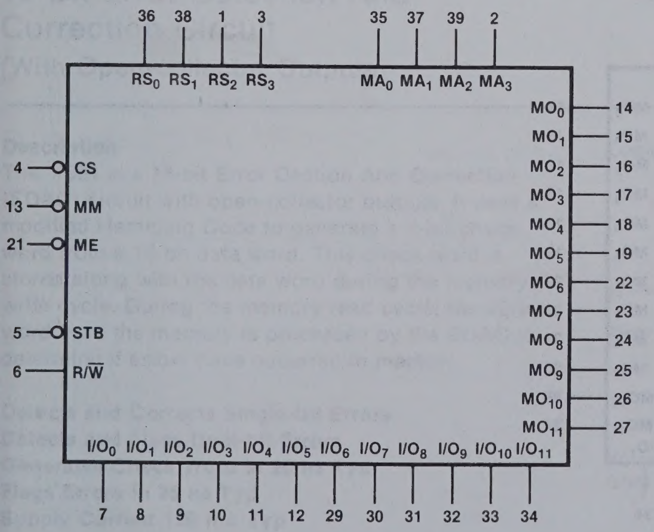
Description

The 'F612 memory mapper is designed to expand the address capability of a Central Processing Unit (CPU) by eight bits. The device contains 16 map registers, each containing 12 bits, that are loaded by the CPU. Subsequently, the four most significant bits of the memory address select one of the 16 registers. The 12 output bits, plus the four least significant memory address bits, form the expanded address. In this mode the 'F612 output stages are transparent. The addressable memory space is increased by periodically reloading the map registers.

In the pass mode the address bits on the register select inputs appear as the most significant bits at the map outputs, with LOW levels appearing on the other bit positions.

Increases Addressing Capability by Eight Bits
Designed for Paged Memory Mapping
3-State Outputs

Logic Symbol


36
38
1
3
35
37
39
2
RS0 RS1 RS2 RS3
MA0 MA1 MA2 MA3
4
CS
13
MM
21
ME
5
STB
6
R/W̄
MO0 14
MO1 15
MO2 16
MO3 17
MO4 18
MO5 19
MO6 22
MO7 23
MO8 24
MO9 25
MO10 26
MO11 27
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8 I/O9 I/O10 I/O11
7
8
9
10
11
12
29
30
31
32
33
34

Vcc = Pin 40
GND = Pin 20

54F/74F613

Memory Mapper
(With Open-collector Outputs)

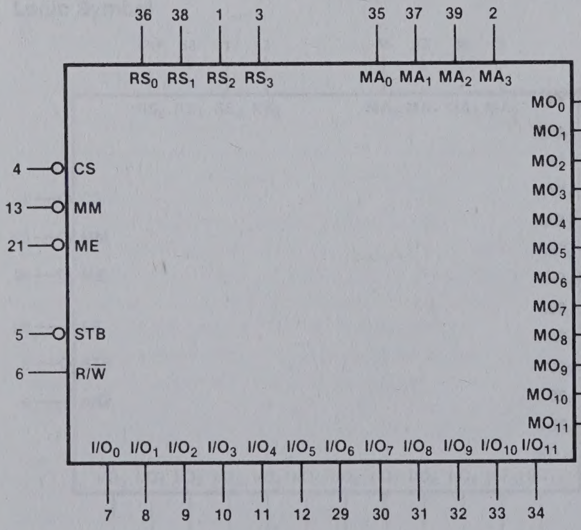
Description

The 'F613 memory mapper is designed to expand the address capability of a Central Processing Unit (CPU) by eight bits. The device contains 16 map registers, each containing 12 bits, that are loaded by the CPU. Subsequently, the four most significant bits of the memory address select one of the 16 registers. The 12 output bits, plus the four least significant memory address bits, form the expanded address. In this mode the 'F613 output stages are transparent. The addressable memory space is increased by periodically reloading the map registers.

In the pass mode the address bits on the register select inputs appear as the most significant bits at the map outputs, with LOW levels appearing on the other bit positions.

Increases Addressing Capability by Eight Bits
Designed for Paged Memory Mapping
Open-collector Outputs

Logic Symbol


36
38
1
3
35
37
39
2
RS_0
RS_1
RS_2
RS_3
MA_0
MA_1
MA_2
MA_3
4
CS
13
MM
21
ME
5
STB
6
R/$\overline{W}$
MO_0 14
MO_1 15
MO_2 16
MO_3 17
MO_4 18
MO_5 19
MO_6 22
MO_7 23
MO_8 24
MO_9 25
MO_{10} 26
MO_{11} 27
I/O_0 I/O_1 I/O_2 I/O_3 I/O_4 I/O_5 I/O_6 I/O_7 I/O_8 I/O_9 I/O_{10} I/O_{11}
7 8 9 10 11 12 29 30 31 32 33 34

V_{CC} = Pin 40
GND = Pin 20

54F/74F630

16-Bit Error Detection And Correction Circuit

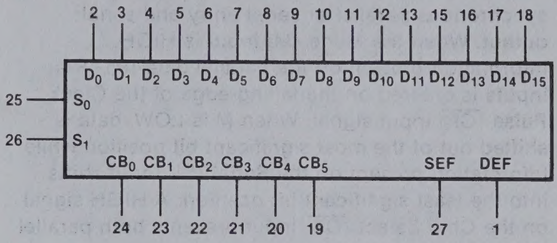
(With 3-State Outputs)

Description

The 'F630 is a 16-bit Error Detection And Correction (EDAC) circuit with 3-state outputs. It uses a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit word from the memory is processed by the EDAC to determine if errors have occurred in memory.

Detects and Corrects Single-bit Errors
Detects and Flags Dual-bit Errors
Generates Check Word in 20 ns Typ
Flags Errors in 25 ns Typ
Supply Current 120 mA Typ

Logic Symbol


2 3 4 5 6 7 8 9 10 11 12 13 15 16 17 18
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
25 S0
26 S1
CB0 CB1 CB2 CB3 CB4 CB5 SEF DEF
24 23 22 21 20 19 27 1

V_{CC} = Pin 28
GND = Pin 14

54F/74F631

16-Bit Error Detection And Correction Circuit

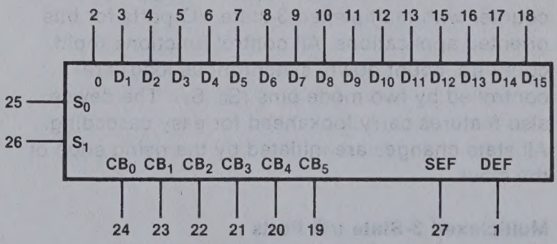
(With Open-collector Outputs)

Description

The 'F631 is a 16-bit Error Dection And Correction (EDAC) circuit with open-collector outputs. It uses a modified Hamming Code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit word from the memory is processed by the EDAC to determine if errors have occurred in memory.

Detects and Corrects Single-bit Errors
Detects and Flags Dual-bit Errors
Generates Check Word in 20 ns Typ
Flags Errors in 25 ns Typ
Supply Current 120 mA Typ

Logic Symbol


2 3 4 5 6 7 8 9 10 11 12 13 15 16 17 18
0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
25 S0
26 S1
CB0 CB1 CB2 CB3 CB4 CB5 SEF DEF
24 23 22 21 20 19 27 1

V_{CC} = Pin 28
GND = Pin 14

54F/74F676

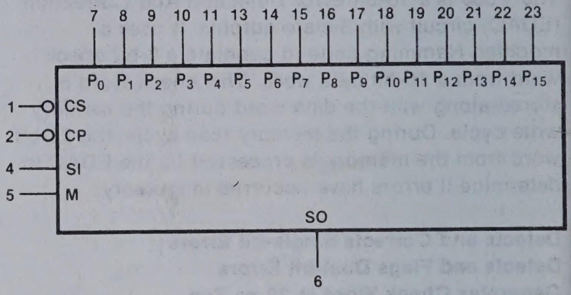
16-Bit Shift Register (Serial/Parallel In, Serial Out)

Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data ($P_0 - P_{15}$) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

16-Bit Parallel-to-Serial Conversion
16-Bit Serial-in, Serial-out
Chip Select Control
Power Supply Current 53 mA Typ
Shift Frequency 100 MHz Typ

Logic Symbol


7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23
P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15
1 CS
2 CP
4 SI
5 M
SO
6

V_{CC} = Pin 24
GND = Pin 12

54F/74F779

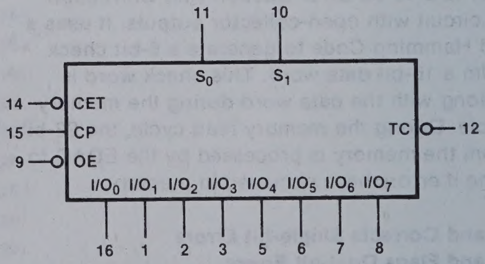
8-Bit Bidirectional Binary Counter

Description

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

Multiplexed 3-State I/O Ports
16-Pin Package for High Packaging Density
Built-in Lookahead Carry Capability
Count Frequency 100 MHz Typ
Supply Current 80 mA Typ

Logic Symbol


11 10
S0 S1
14 CET
15 CP
9 OE
TC 12
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7
16 1 2 3 5 6 7 8

V_{CC} = Pin 13
GND = Pin 4

54F/74F784

8-Bit Serial/Parallel Multiplier

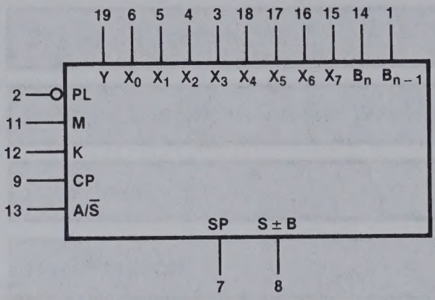
(With Adder/Subtractor)

Description

The 'F784 is a serial n x 8-bit multiplier with a final stage adder/subtractor for optional use in adding a B bit to obtain S ± B. A 'B - 1' bit can also be added via an internal flip-flop to achieve a 1-bit delay. The x word is parallel loaded (eight bits wide) into latches and the y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in fast Fourier transforms.

Twos Complement Multiplication
Cascadable for any Number of Bits
Full Adder and B - 1 Input Included for Maximum Flexibility
Maximum Clock Frequency 100 MHz Typ
Supply Current 78 mA Typ

Logic Symbol


19
6
5
4
3
18
17
16
15
14
1
Y
X_0
X_1
X_2
X_3
X_4
X_5
X_6
X_7
B_n
B_{n-1}
2
PL
11
M
12
K
9
CP
13
$A/\overline{S}$
SP
S ± B
7
8

V_{CC} = Pin 20
GND = Pin 10

54F/74F676

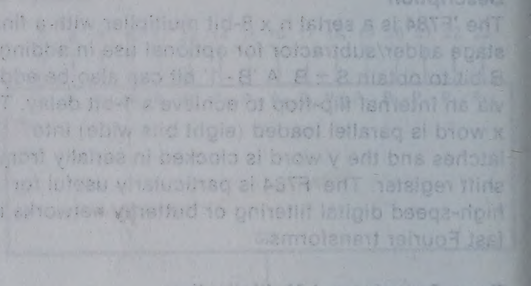
16-Bit Shift Register (Serial/Parallel In, Serial Out)

Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. [illegible] information present on the parallel data (P0–P15) inputs is entered on the falling edge of the Clock Pulse (CP) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select (CS) input prevents both parallel and serial operations.

- 16-Bit Parallel-to-Serial Conversion
- 16-Bit Serial-In, Serial-Out
- Chip Select Control
- Power Supply Current 68 mA Typ
- Shift Frequency 100 MHz Typ

Logic Symbol



Vcc = Pin 24
GND = Pin 12

54F/74F779

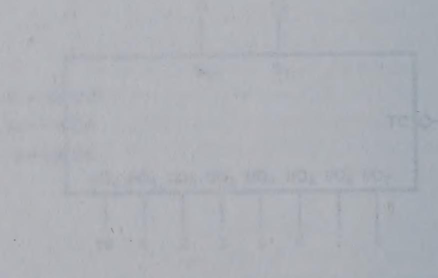
8-Bit Bidirectional Binary Counter

Description

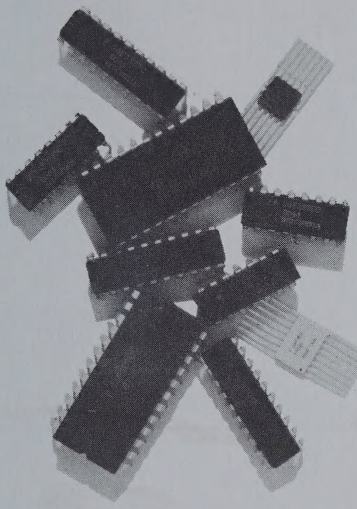
The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S0, S1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

- Multiplexed 3-State I/O Ports
- 16-Pin Package for High Packaging Density
- Built-In Lookahead Carry Capability
- Count Frequency 100 MHz Typ
- Supply Current 80 mA Typ

Logic Symbol


TC
15
I/O_0 I/O_1 I/O_2 I/O_3 I/O_4 I/O_5 I/O_6 I/O_7

Vcc = Pin 16
GND = Pin 8



Product Index and Selection Guide 1

Circuit Characteristics 2

Ratings, Specifications and Waveforms 3

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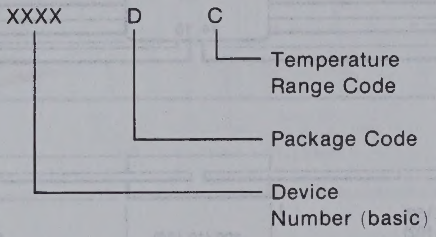
Section 6

Ordering Information/ Package Outlines

Specific ordering codes, as well as the temperature ranges and package types available, are listed on each data sheet in Section 4. The Product Index and Selection Guide given in Section 1 list only the "basic device numbers." This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Temperature Range — Two basic temperature grades are in common use:

C = Commercial
0°C to +70°C
M = Military
-55°C to +125°C

Package Code — One letter represents the basic package type. Different package outlines exist within each package type to accommodate varying die sizes and number of pins, as indicated below:

D — Ceramic/Hermetic Dual In-line
4E, 6A, 6B, 6N, 7B, 8S

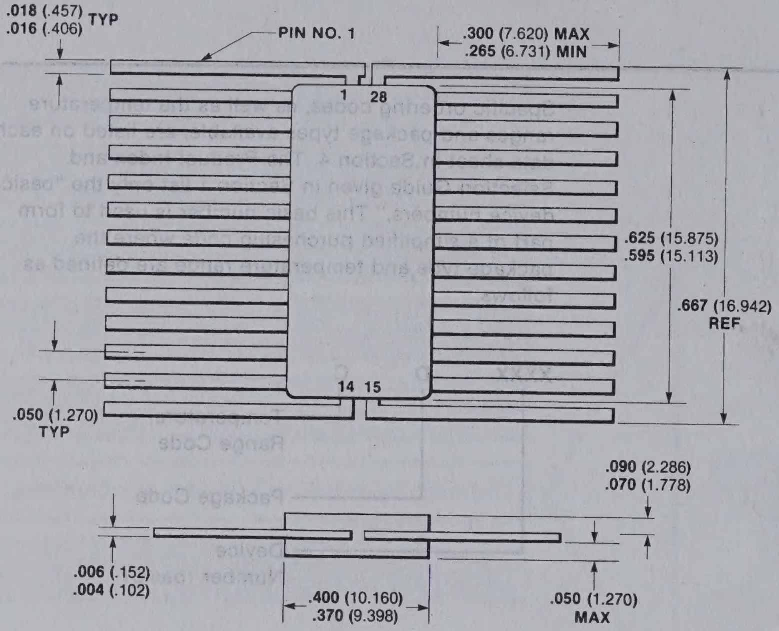
F — Flatpak
2E, 3I, 4D, 4L, 4M, 4W

P — Plastic Dual In-line
9A, 9B, 9L, 9N, 9Y, 9Z

Package Outlines — The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

2E

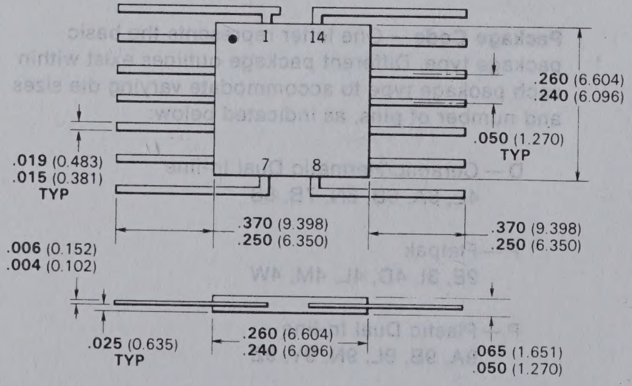
28-Pin Ceramic Flatpak


.018 (.457)
.016 (.406) TYP
PIN NO. 1
.300 (7.620) MAX
.265 (6.731) MIN
1
28
14
15
.625 (15.875)
.595 (15.113)
.667 (16.942)
REF
.050 (1.270)
TYP
.090 (2.286)
.070 (1.778)
.006 (.152)
.004 (.102)
.400 (10.160)
.370 (9.398)
.050 (1.270)
MAX

Notes
Pins are tin plated alloy 42 or equivalent
Base and cap are alumina, black
Cavity size is **.200 × .300** (5.08 × 7.62)
Package weight is 1.0 gram

3I

14-Pin Ceramic Flatpak

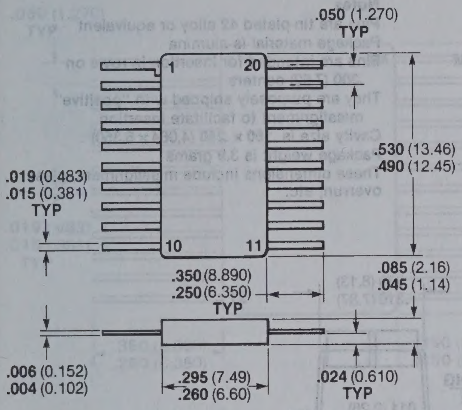

1
14
7
8
.260 (6.604)
.240 (6.096)
.050 (1.270)
TYP
.019 (0.483)
.015 (0.381)
TYP
.370 (9.398)
.250 (6.350)
.370 (9.398)
.250 (6.350)
.006 (0.152)
.004 (0.102)
.025 (0.635)
TYP
.260 (6.604)
.240 (6.096)
.065 (1.651)
.050 (1.270)

Notes
Pins are tin-plated 42 alloy
Hermetically sealed alumina package
Pin 1 orientation may be either tab or dot
Cavity size is **.130 × .130** (3.30 × 3.30)
Package weight is 0.26 gram

All dimensions are in inches **bold** and (millimeters)

4D

20-Pin Ceramic Flatpak


.050 (1.270)
TYP
1
20
.530 (13.46)
.490 (12.45)
.019 (0.483)
.015 (0.381)
TYP
10
11
.085 (2.16)
.045 (1.14)
.350 (8.890)
.250 (6.350)
TYP
.006 (0.152)
.004 (0.102)
.295 (7.49)
.260 (6.60)
.024 (0.610)
TYP

Notes

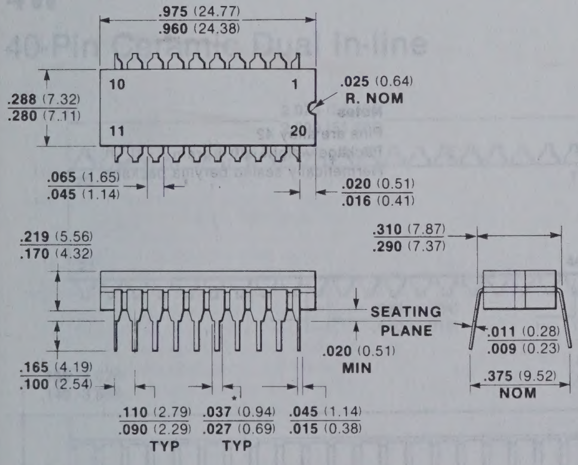
Pins are tin-plated alloy 42

Cap and base are Al_2O_3

Package weight is 0.8 gram

4E

20-Pin Ceramic Dual In-line


.975 (24.77)
.960 (24.38)
10
1
.025 (0.64)
R. NOM
.288 (7.32)
.280 (7.11)
11
20
.065 (1.65)
.045 (1.14)
.020 (0.51)
.016 (0.41)
.219 (5.56)
.170 (4.32)
.310 (7.87)
.290 (7.37)
SEATING
PLANE
.011 (0.28)
.009 (0.23)
.020 (0.51)
MIN
.165 (4.19)
.100 (2.54)
.375 (9.52)
NOM
.110 (2.79)
.090 (2.29)
TYP
*
.037 (0.94)
.027 (0.69)
TYP
.045 (1.14)
.015 (0.38)

Notes

Pins are tin-plated kovar or nickel alloy 42

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for **.030** (0.76) diameter pins

Hermetically sealed alumina package (black)

Cavity size is **.140 x .250** (3.56 x 6.35)

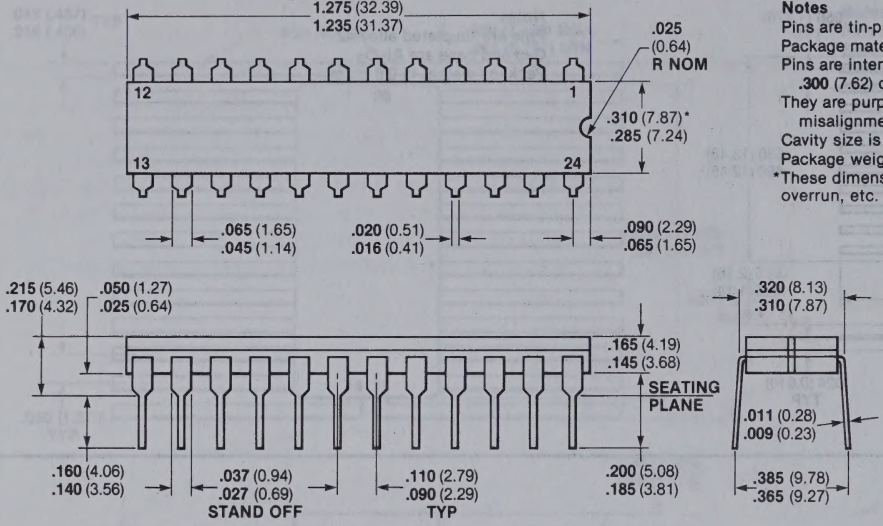
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins

Package weight is 2.4 grams

All dimensions are in inches **bold** and (millimeters)

4H

24-Pin Slim Ceramic Dual In-line

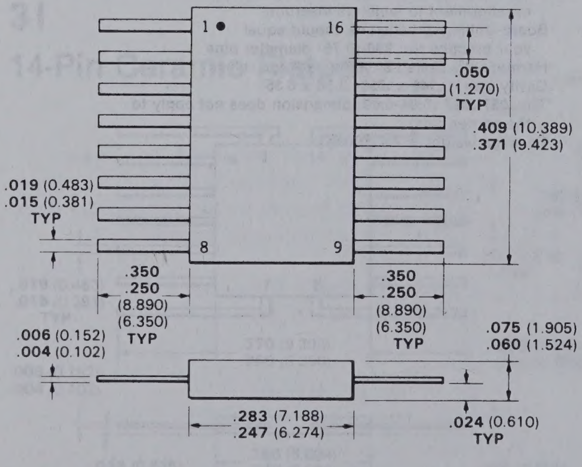

1.275 (32.39)
1.235 (31.37)
.025
(0.64)
R NOM
12
1
13
24
.310 (7.87)*
.285 (7.24)
.065 (1.65)
.045 (1.14)
.020 (0.51)
.016 (0.41)
.090 (2.29)
.065 (1.65)
.215 (5.46)
.170 (4.32)
.050 (1.27)
.025 (0.64)
.165 (4.19)
.145 (3.68)
SEATING
PLANE
.320 (8.13)
.310 (7.87)
.011 (0.28)
.009 (0.23)
.160 (4.06)
.140 (3.56)
.037 (0.94)
.027 (0.69)
STAND OFF
.110 (2.79)
.090 (2.29)
TYP
.200 (5.08)
.185 (3.81)
.385 (9.78)
.365 (9.27)

Notes

Pins are tin-plated 42 alloy or equivalent
Package material is alumina
Pins are intended for insertion in rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.160 × .250** (4.064 × 6.350)
Package weight is 3.9 grams
*These dimensions include misalignment, glass overrun, etc.

4L

16-Pin Ceramic Flatpak

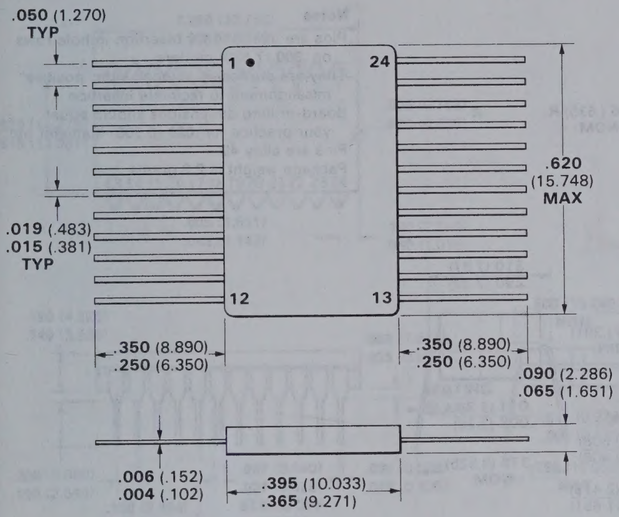

1 ●
16
8
9
.050
(1.270)
TYP
.409 (10.389)
.371 (9.423)
.019 (0.483)
.015 (0.381)
TYP
.350
.250
(8.890)
(6.350)
TYP
.350
.250
(8.890)
(6.350)
TYP
.006 (0.152)
.004 (0.102)
.075 (1.905)
.060 (1.524)
.283 (7.188)
.247 (6.274)
.024 (0.610)
TYP

Notes

Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

4M

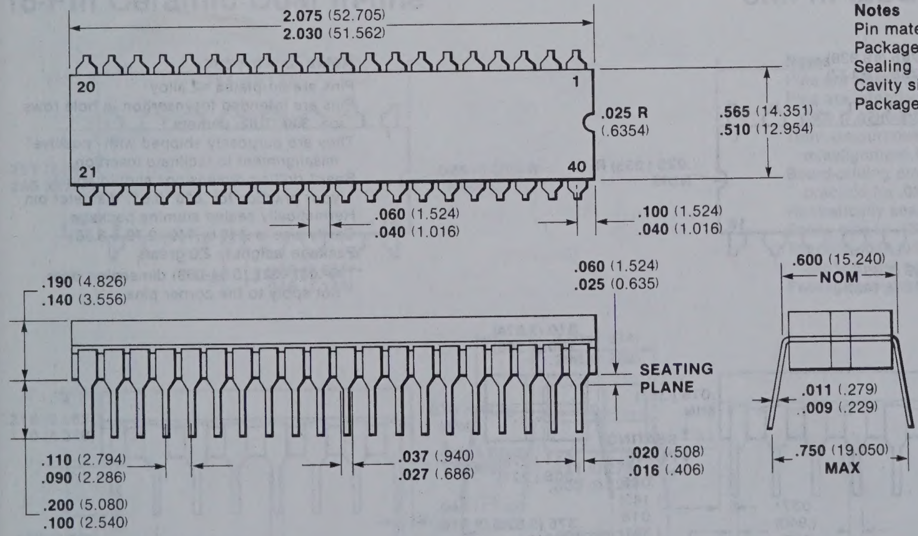
24-Pin Ceramic Flatpak


.050 (1.270)
TYP
1
24
12
13
.620
(15.748)
MAX
.019 (.483)
.015 (.381)
TYP
.350 (8.890)
.250 (6.350)
.350 (8.890)
.250 (6.350)
.090 (2.286)
.065 (1.651)
.006 (.152)
.004 (.102)
.395 (10.033)
.365 (9.271)

Notes
Pins are tin-plated 42 alloy
Cap material is alumina
Base material is beryllia
Cavity size is **.222** x **.250** (5.64 x 6.35)
Package weight is 0.8 gram

4W

40-Pin Ceramic Dual In-line

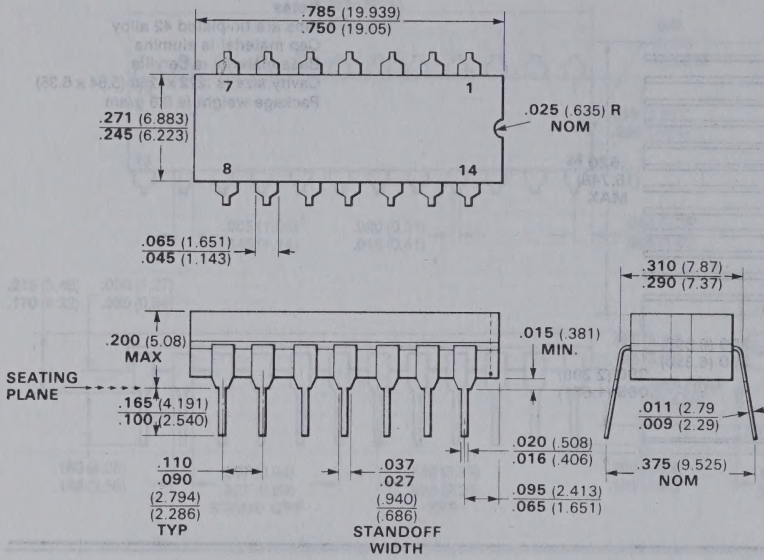

2.075 (52.705)
2.030 (51.562)
20
1
21
40
.025 R
(.6354)
.565 (14.351)
.510 (12.954)
.060 (1.524)
.040 (1.016)
.100 (1.524)
.040 (1.016)
.190 (4.826)
.140 (3.556)
.060 (1.524)
.025 (0.635)
SEATING
PLANE
.600 (15.240)
NOM
.011 (.279)
.009 (.229)
.750 (19.050)
MAX
.110 (2.794)
.090 (2.286)
.037 (.940)
.027 (.686)
.020 (.508)
.016 (.406)
.200 (5.080)
.100 (2.540)

Notes
Pin material is kovar
Package material is alumina
Sealing material is vitreous glass
Cavity size is **.260** x **.270** (6.604 x 6.858)
Package weight is 12 grams

All dimensions are in inches **bold** and (millimeters)

6A

14-Pin Ceramic Dual In-line



.785 (19.939)
.750 (19.05)
7
1
8
14
.271 (6.883)
.245 (6.223)
.025 (.635) R
NOM
.065 (1.651)
.045 (1.143)
.310 (7.87)
.290 (7.37)
.200 (5.08)
MAX
SEATING
PLANE
.015 (.381)
MIN.
.165 (4.191)
.100 (2.540)
.011 (2.79
.009 (2.29)
.020 (.508)
.016 (.406)
.110
.090
(2.794)
(2.286)
TYP
.037
.027
(.940)
(.686)
STANDOFF
WIDTH
.375 (9.525)
NOM
.095 (2.413)
.065 (1.651)

Notes

Pins are intended for insertion in hole rows on **.300** (7.620) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

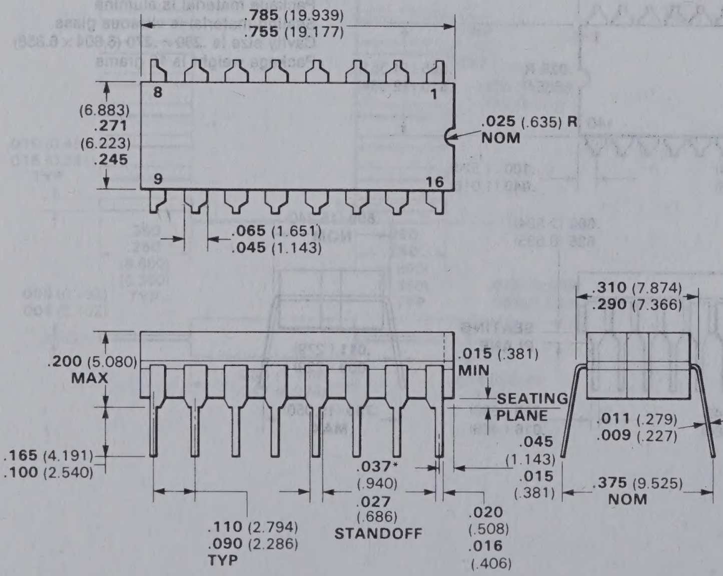
Board-drilling dimensions should equal your practice for **.020** (0.508) diameter pin

Pins are alloy 42

Package weight is 2.0 grams

6B

16-Pin Ceramic Dual In-line



.785 (19.939)
.755 (19.177)
8
1
9
16
(6.883)
.271
(6.223)
.245
.025 (.635) R
NOM
.065 (1.651)
.045 (1.143)
.310 (7.874)
.290 (7.366)
.200 (5.080)
MAX
.015 (.381)
MIN
SEATING
PLANE
.045
(1.143)
.015
(.381)
.011 (.279)
.009 (.227)
.165 (4.191)
.100 (2.540)
.037*
(.940)
.027
(.686)
STANDOFF
.375 (9.525)
NOM
.110 (2.794)
.090 (2.286)
TYP
.020
(.508)
.016
(.406)

Notes

Pins are tin-plated 42 alloy

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin

Hermetically sealed alumina package

Cavity size is **.110 x .140** (2.79 x 3.56)

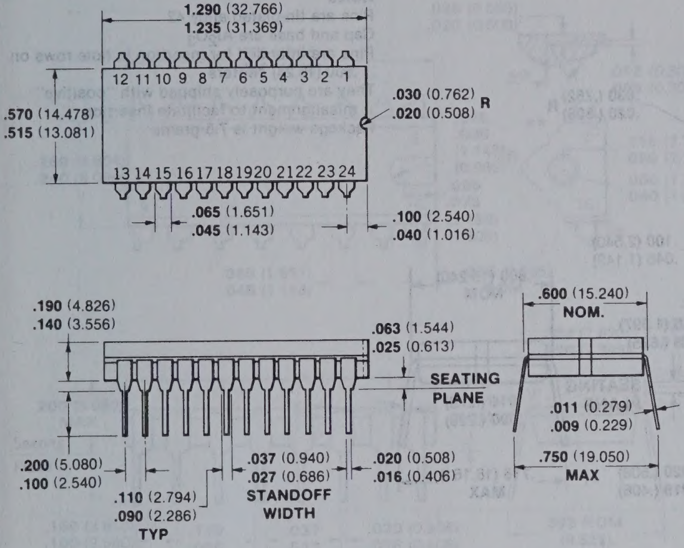
Package weight is 2.0 grams

*The **.037-.027** (0.94-069) dimension does not apply to the corner pins

All dimensions are in inches **bold** and (millimeters)

6N

24-Pin Ceramic Dual In-line


1.290 (32.766)
1.235 (31.369)
12 11 10 9 8 7 6 5 4 3 2 1
.570 (14.478)
.515 (13.081)
.030 (0.762)
.020 (0.508)
R
13 14 15 16 17 18 19 20 21 22 23 24
.065 (1.651)
.045 (1.143)
.100 (2.540)
.040 (1.016)
.190 (4.826)
.140 (3.556)
.063 (1.544)
.025 (0.613)
SEATING PLANE
.600 (15.240)
NOM.
.011 (0.279)
.009 (0.229)
.200 (5.080)
.100 (2.540)
.110 (2.794)
.090 (2.286)
TYP
.037 (0.940)
.027 (0.686)
STANDOFF WIDTH
.020 (0.508)
.016 (0.406)
.750 (19.050)
MAX

Notes

Pins are tin-plated 42 alloy

Package material is alumina

Pins are intended for insertion in hole rows on **.600** (15.24) centers

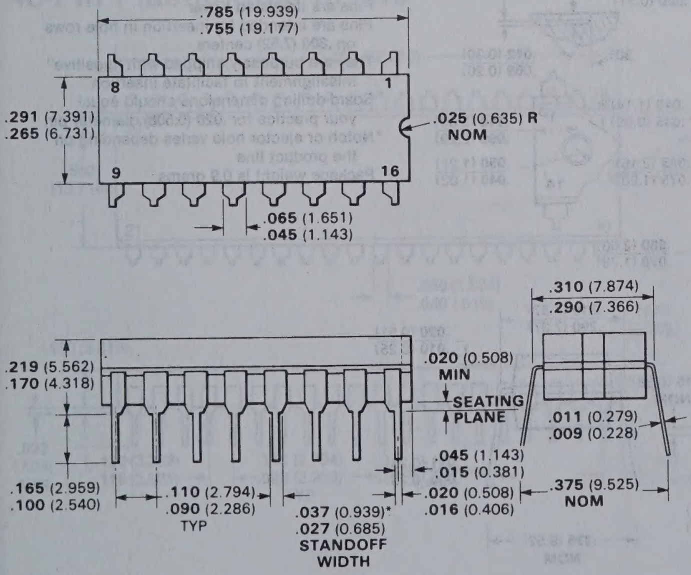
They are purposely shipped with "positive" misalignment to facilitate insertion

Cavity size is **.230 x .230** (5.84 x 5.84)

Package weight is 6.5 grams

7B

16-Pin Ceramic Dual In-line


.785 (19.939)
.755 (19.177)
8
1
.291 (7.391)
.265 (6.731)
.025 (0.635) R
NOM
9
16
.065 (1.651)
.045 (1.143)
.310 (7.874)
.290 (7.366)
.219 (5.562)
.170 (4.318)
.020 (0.508)
MIN
SEATING PLANE
.011 (0.279)
.009 (0.228)
.045 (1.143)
.015 (0.381)
.165 (2.959)
.100 (2.540)
.110 (2.794)
.090 (2.286)
TYP
.020 (0.508)
.016 (0.406)
.375 (9.525)
NOM
.037 (0.939)*
.027 (0.685)
STANDOFF WIDTH

Notes

Pins are tin-plated 42 alloy

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin

Hermetically sealed alumina package

Cavity size is **.130 x .230** (3.302 x 5.842)

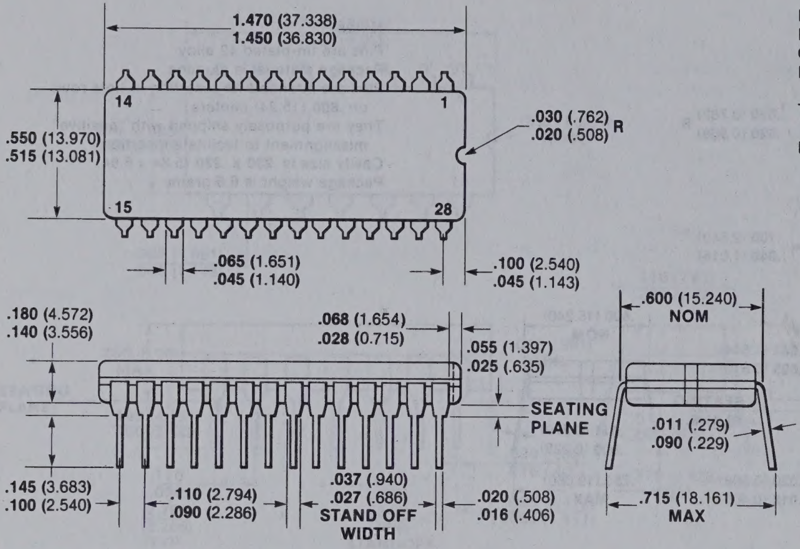
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins

Package weight is 2.2 grams

All dimensions are in inches **bold** and (millimeters)

8S

28-Pin Ceramic Dual In-line


1.470 (37.338)
1.450 (36.830)
14
1
.550 (13.970)
.515 (13.081)
.030 (.762)
.020 (.508) R
15
28
.065 (1.651)
.045 (1.140)
.100 (2.540)
.045 (1.143)
.600 (15.240)
NOM
.180 (4.572)
.140 (3.556)
.068 (1.654)
.028 (0.715)
.055 (1.397)
.025 (.635)
SEATING
PLANE
.011 (.279)
.090 (.229)
.145 (3.683)
.100 (2.540)
.110 (2.794)
.090 (2.286)
.037 (.940)
.027 (.686)
STAND OFF
WIDTH
.020 (.508)
.016 (.406)
.715 (18.161)
MAX

Notes

Pins are tin-plated alloy 42

Cap and base are Al_2O_3

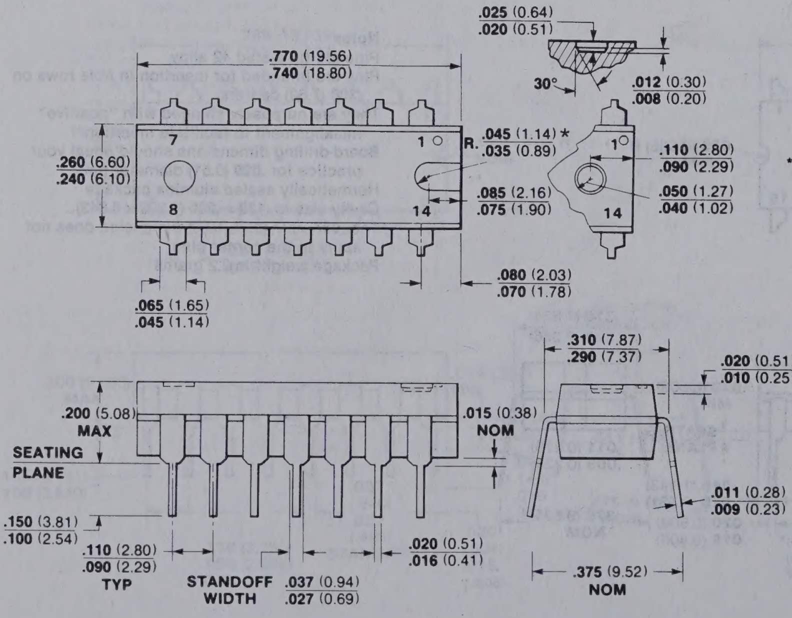
Pins are intended for insertion in hole rows on **.600** (15.24) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Package weight is 7.5 grams

9A

14-Pin Plastic Dual In-line


.025 (0.64)
.020 (0.51)
.770 (19.56)
.740 (18.80)
30°
.012 (0.30)
.008 (0.20)
7
1
R. .045 (1.14) *
.035 (0.89)
1
.110 (2.80)
.090 (2.29)
.260 (6.60)
.240 (6.10)
.085 (2.16)
.075 (1.90)
.050 (1.27)
.040 (1.02)
8
14
14
.080 (2.03)
.070 (1.78)
.065 (1.65)
.045 (1.14)
.310 (7.87)
.290 (7.37)
.020 (0.51)
.010 (0.25)
.200 (5.08)
MAX
.015 (0.38)
NOM
SEATING
PLANE
.011 (0.28)
.009 (0.23)
.150 (3.81)
.100 (2.54)
.110 (2.80)
.090 (2.29)
TYP
.020 (0.51)
.016 (0.41)
STANDOFF
WIDTH
.037 (0.94)
.027 (0.69)
.375 (9.52)
NOM

Notes

Pins are tin-plated Kovar

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for **.020** (0.508) diameter pin

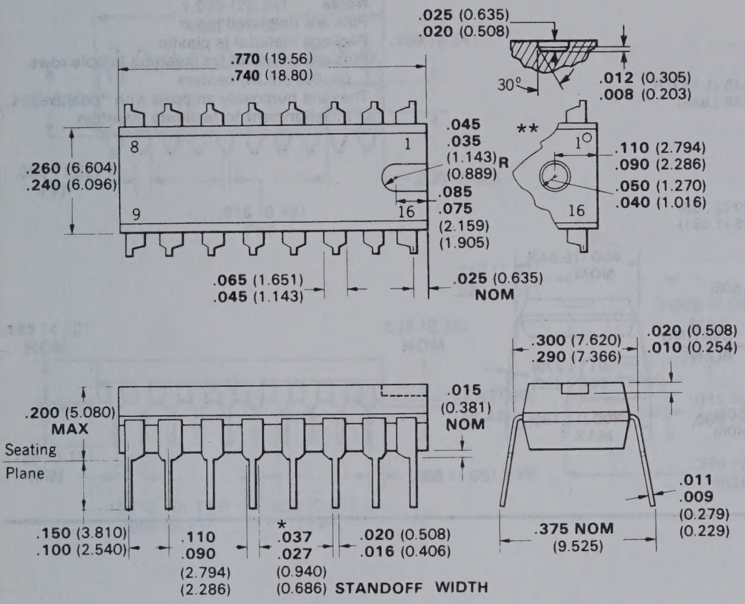
*Notch or ejector hole varies depending on the product line

Package weight is 0.9 grams

All dimensions are in inches **bold** and (millimeters)

9B

16-Pin Plastic Dual In-line


.025 (0.635)
.020 (0.508)
.770 (19.56)
.740 (18.80)
30°
.012 (0.305)
.008 (0.203)
8
1
.045
.035
(1.143)R
(0.889)
**
1
.110 (2.794)
.090 (2.286)
.260 (6.604)
.240 (6.096)
.085
.075
(2.159)
(1.905)
.050 (1.270)
.040 (1.016)
9
16
16
.065 (1.651)
.045 (1.143)
.025 (0.635)
NOM
.300 (7.620)
.290 (7.366)
.020 (0.508)
.010 (0.254)
.200 (5.080)
MAX
.015
(0.381)
NOM
Seating
Plane
.011
.009
(0.279)
(0.229)
.150 (3.810)
.100 (2.540)
.110
.090
(2.794)
(2.286)
*
.037
.027
(0.940)
(0.686) STANDOFF WIDTH
.020 (0.508)
.016 (0.406)
.375 NOM
(9.525)

Notes

Pins are tin-plated kovar or alloy 42 nickel

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board drilling dimensions should equal your practice for **.0210** (0.51) diameter pin

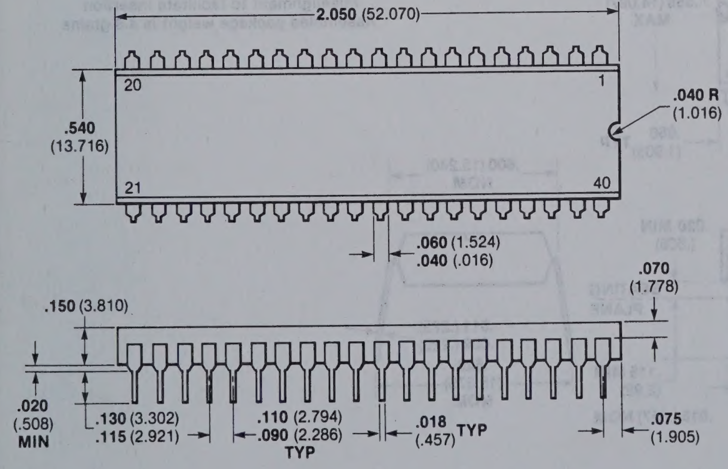
*The **.037-0.27** (0.94-0.69) dimension does not apply to the corner pins

**Notch or ejector hole varies depending on the product line

Package weight is 0.9 grams

9L

40-Pin Plastic Dual In-line


2.050 (52.070)
20
1
.540
(13.716)
.040 R
(1.016)
21
40
.060 (1.524)
.040 (.016)
.150 (3.810)
.070
(1.778)
.020
(.508)
MIN
.130 (3.302)
.115 (2.921)
.110 (2.794)
.090 (2.286)
TYP
.018
(.457) TYP
.075
(1.905)

Notes

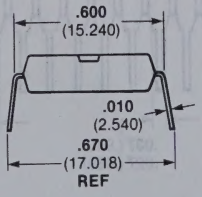
Pins are tin-plated alloy 42

Package material is plastic

Pins are intended for insertion in hole rows on .600 (15.24) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

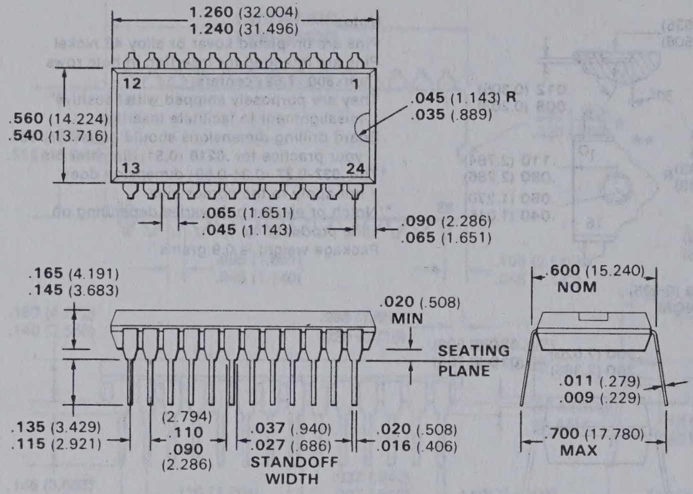
Package weight is 7.0 grams


.600
(15.240)
.010
(2.540)
.670
(17.018)
REF

All dimensions are in inches **bold** and (millimeters)

9N

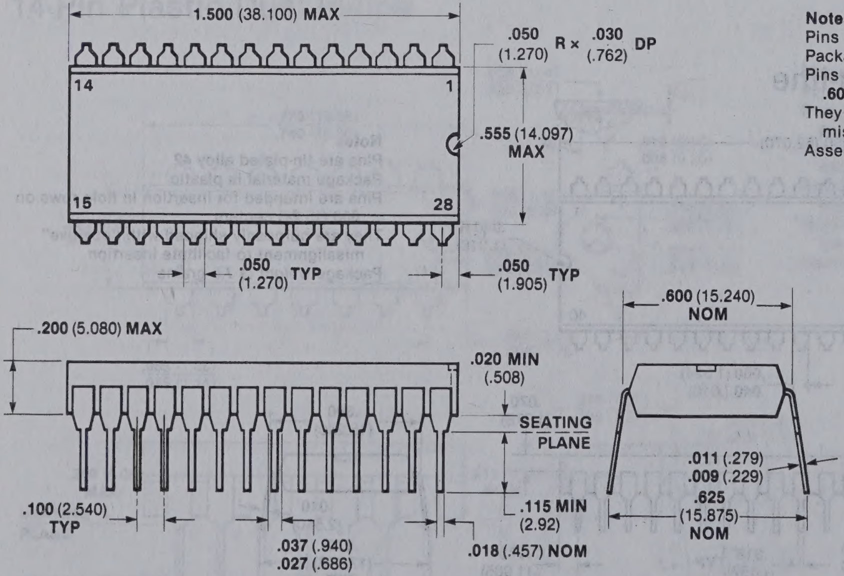
24-Pin Plastic Dual In-line


1.260 (32.004)
1.240 (31.496)
12
1
13
24
.560 (14.224)
.540 (13.716)
.045 (1.143) R
.035 (.889)
.065 (1.651)
.045 (1.143)
.090 (2.286)
.065 (1.651)
.165 (4.191)
.145 (3.683)
.020 (.508)
MIN
SEATING
PLANE
.135 (3.429)
.115 (2.921)
(2.794)
.110
.090
(2.286)
.037 (.940)
.027 (.686)
STANDOFF
WIDTH
.020 (.508)
.016 (.406)
.600 (15.240)
NOM
.011 (.279)
.009 (.229)
.700 (17.780)
MAX

Notes
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

9Y

28-Pin Plastic Dual In-line

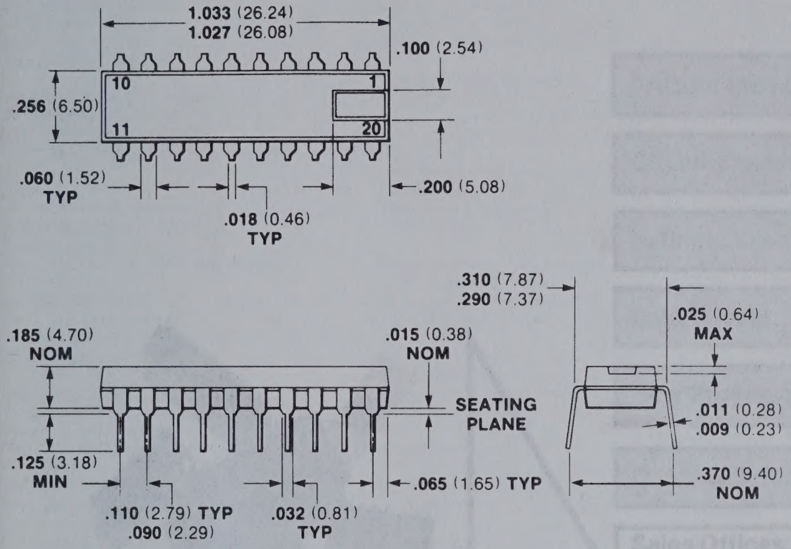

1.500 (38.100) MAX
.050
(1.270)
R ×
.030
(.762)
DP
14
1
15
28
.555 (14.097)
MAX
.050
(1.270)
TYP
.050
(1.905)
TYP
.200 (5.080) MAX
.020 MIN
(.508)
SEATING
PLANE
.115 MIN
(2.92)
.100 (2.540)
TYP
.037 (.940)
.027 (.686)
.018 (.457) NOM
.600 (15.240)
NOM
.011 (.279)
.009 (.229)
.625
(15.875)
NOM

Notes
Pins are tin-plated kovar, alloy 42 or copper
Package material is plastic
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Assembled package weight is 4.8 grams

All dimensions are in inches **bold** and (millimeters)

9Z

20-Pin Plastic Dual In-line


1.033 (26.24)
1.027 (26.08)
.100 (2.54)
10
1
.256 (6.50)
11
20
.060 (1.52) TYP
.200 (5.08)
.018 (0.46) TYP
.310 (7.87)
.290 (7.37)
.025 (0.64) MAX
.185 (4.70) NOM
.015 (0.38) NOM
SEATING PLANE
.011 (0.28)
.009 (0.23)
.125 (3.18) MIN
.065 (1.65) TYP
.370 (9.40) NOM
.110 (2.79) TYP
.090 (2.29)
.032 (0.81) TYP

Notes

Pins are tin-plated alloy 42 copper (olin 195)

Pins are intended for insertion in hole rows on **.300** (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

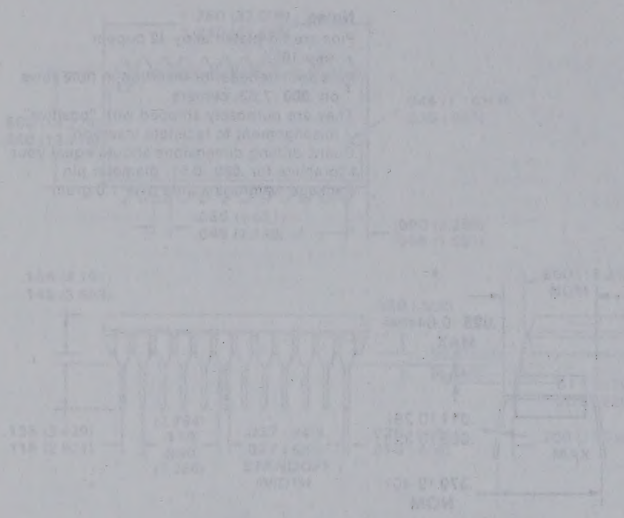
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin

Package weight is a little over 1.0 gram

All dimensions are in inches **bold** and (millimeters)

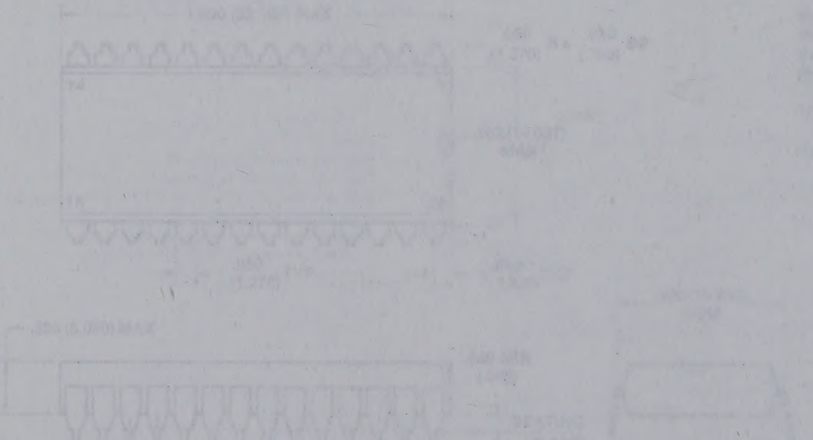
9N

24-Pin Plastic Dual In-line

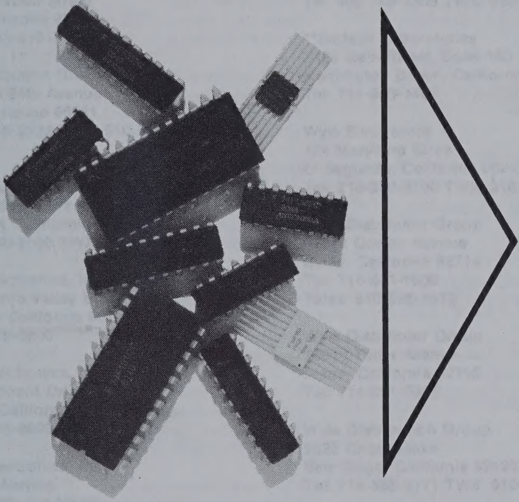


9Y

28-Pin Plastic Dual In-line



Notes
Pins are tin-plated Alloy 42 or copper
Package material is plastic
Pins are intended for insertion in hole rows on
.600 (15.24) centers
They are purposely shipped with "positive"
misalignment to facilitate insertion
Typical package weight is 5.6 grams



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Tempe, Arizona 85281
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Anthem Electronics, Inc.
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Tel: 714-960-1403

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124 Maryland Street
El Segundo, California 90245
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Telex: 910-595-1572

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7705 Maltlage Drive
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Binghampton, New York 13902
(shipping address)
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[illegible] Family DC Characteristics

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	Vcc	Conditions
[illegible]	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended Vcc and TA Range
[illegible]	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended Vcc and TA Range
[illegible]	Input Clamp Diode Voltage				−1.2	V	Min	IIN = −18 mA
[illegible]	Output HIGH Voltage	Std. & Mil	2.5	3.4		V	Min	IOH = [illegible] μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		[illegible] Com	2	3.4				
[illegible]	Output LOW Voltage			0.30	0.5	V	Min	IOL = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
[illegible]	Input HIGH Current	0.5 U.L.			20	μA	Max	IIH = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet, VIN = 2.7 V
		1.0 U.L.			40			
		n U.L.			n × [illegible]			
[illegible]	Input HIGH Current Breakdown Test, All Inputs				100	μA	Max	VIN = 7.0 V
[illegible]	Input LOW Current	0.375 U.L.			−0.6	mA	Max	IIL = −1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet, VIN = 0.5 V
		1.0 U.L.			−1.6			
		n U.L.			n × [illegible]			
[illegible]	3-State Output OFF Current HIGH				50	μA	Max	VOUT = 2.4 V
[illegible]	3-State Output OFF Current LOW				−50	μA	Max	VOUT = 0.5 V
[illegible]	Output Short-Circuit Current	Standard/3-State	−60		−150	mA	Max	VOUT = 0 V
		Buffers/Line Drvs	−100		−225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. [illegible]
2. [illegible]
3. [illegible]
4. [illegible] TA = 25°C and Vcc = 5.0 V.
5. [illegible]
6. [illegible]
7. [illegible]

54F/74F Family DC Characteristics[1]

Symbol	Parameter		Limits[2]			Units	V_{CC}[4]	Conditions[2]
			Min	Typ[3]	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std[6] Mil	2.5	3.4		V	Min	I_{OH} = 40 µA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std[6] Com	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	µA	Max	I_{IH} = 40 µA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				100	µA	Max	V_{IN} = 7.0 V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.5 V
		0.75 U.L.			-1.2			
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				50	µA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-50	µA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short-Circuit Current	Standard[6]/ 3-State	-60		-150	mA	Max	V_{OUT} = 0 V
		Buffers/ Line Dvrs	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

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Printed in U.S.A./2022-839-A-22-100 50M March 1982